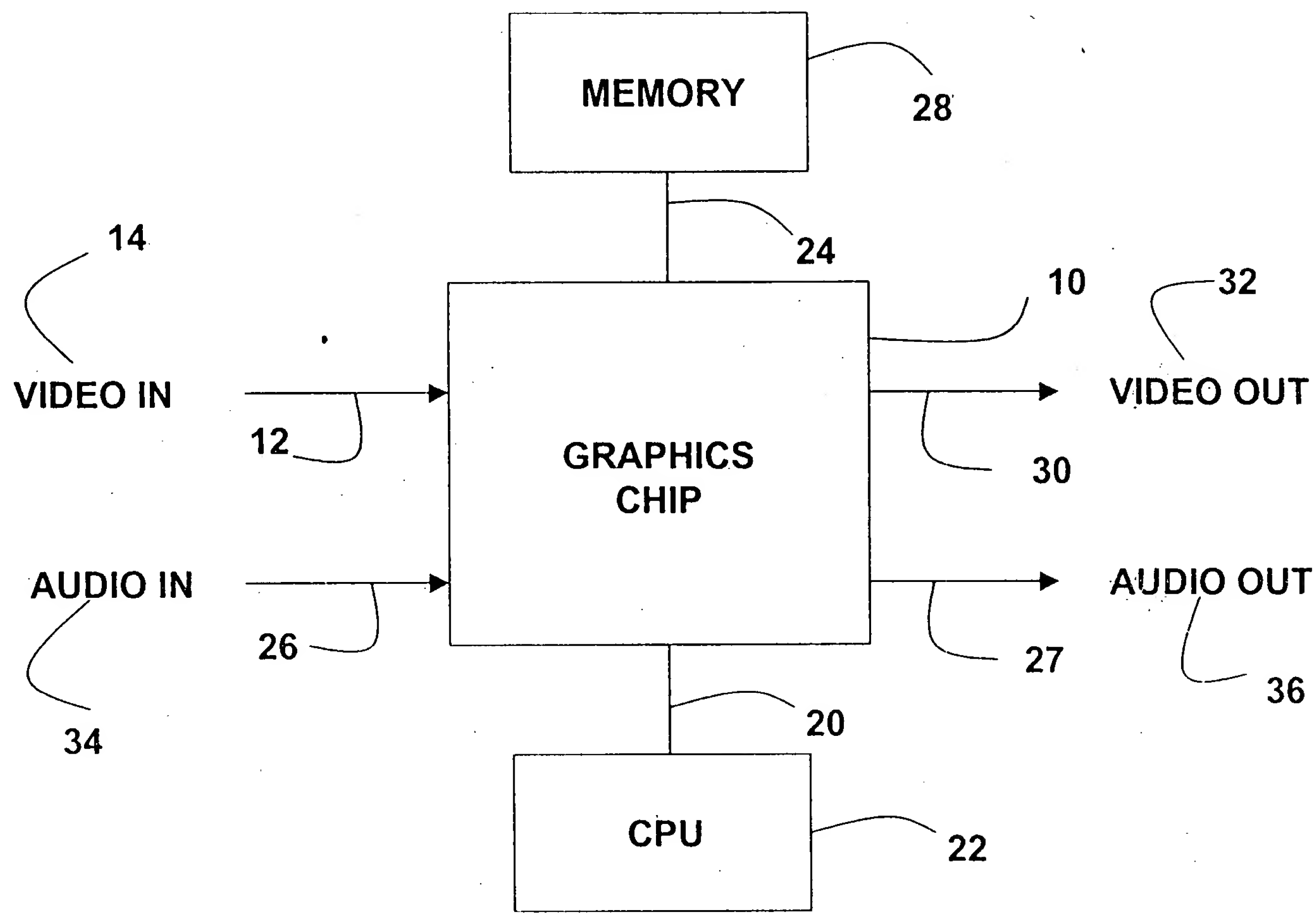

MEMORY
28
24
14
VIDEO IN
12
GRAPHICS CHIP
10
32
VIDEO OUT
30
AUDIO IN
26
AUDIO OUT
27
36
34
20
CPU
22

FIG. 1

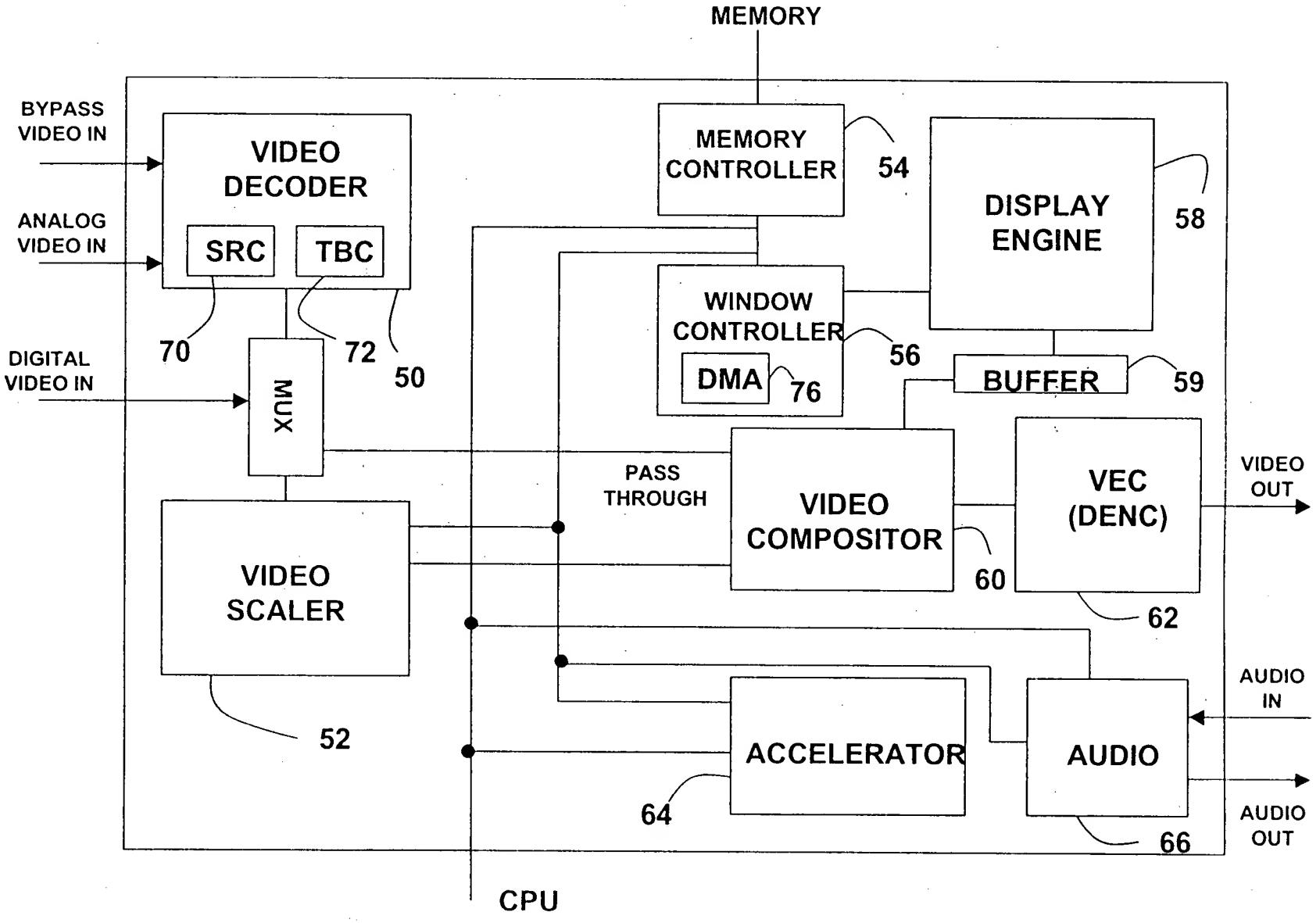

FIG. 2

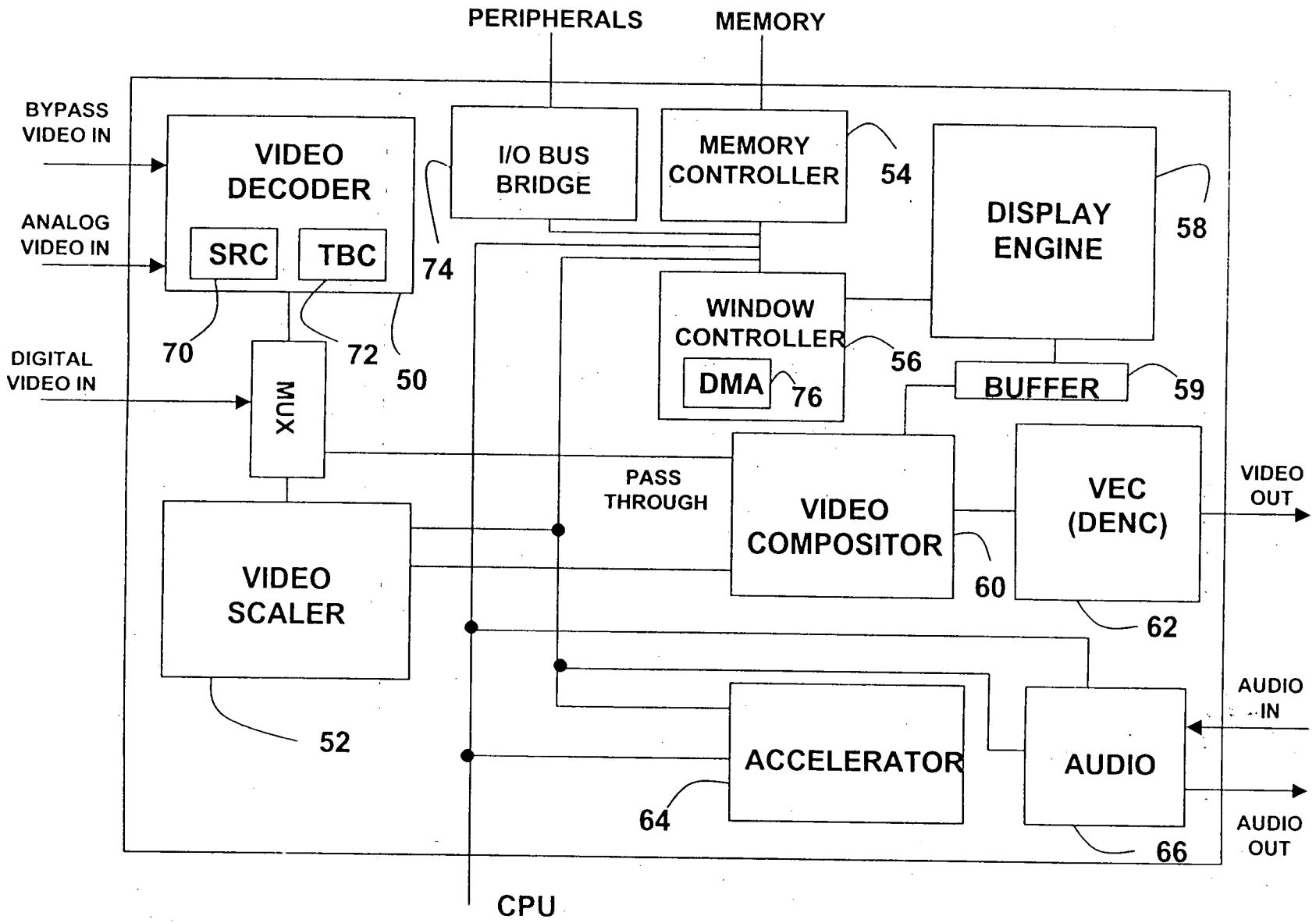
PERIPHERALS
MEMORY
BYPASS VIDEO IN
ANALOG VIDEO IN
DIGITAL VIDEO IN
VIDEO DECODER
SRC
TBC
I/O BUS BRIDGE
MEMORY CONTROLLER
54
DISPLAY ENGINE
58
74
WINDOW CONTROLLER
DMA
76
56
BUFFER
59
70
72
50
MUX
PASS THROUGH
VIDEO COMPOSITOR
60
VEC (DENC)
VIDEO OUT
VIDEO SCALER
62
52
AUDIO IN
ACCELERATOR
64
AUDIO
66
AUDIO OUT
CPU

FIG. 3

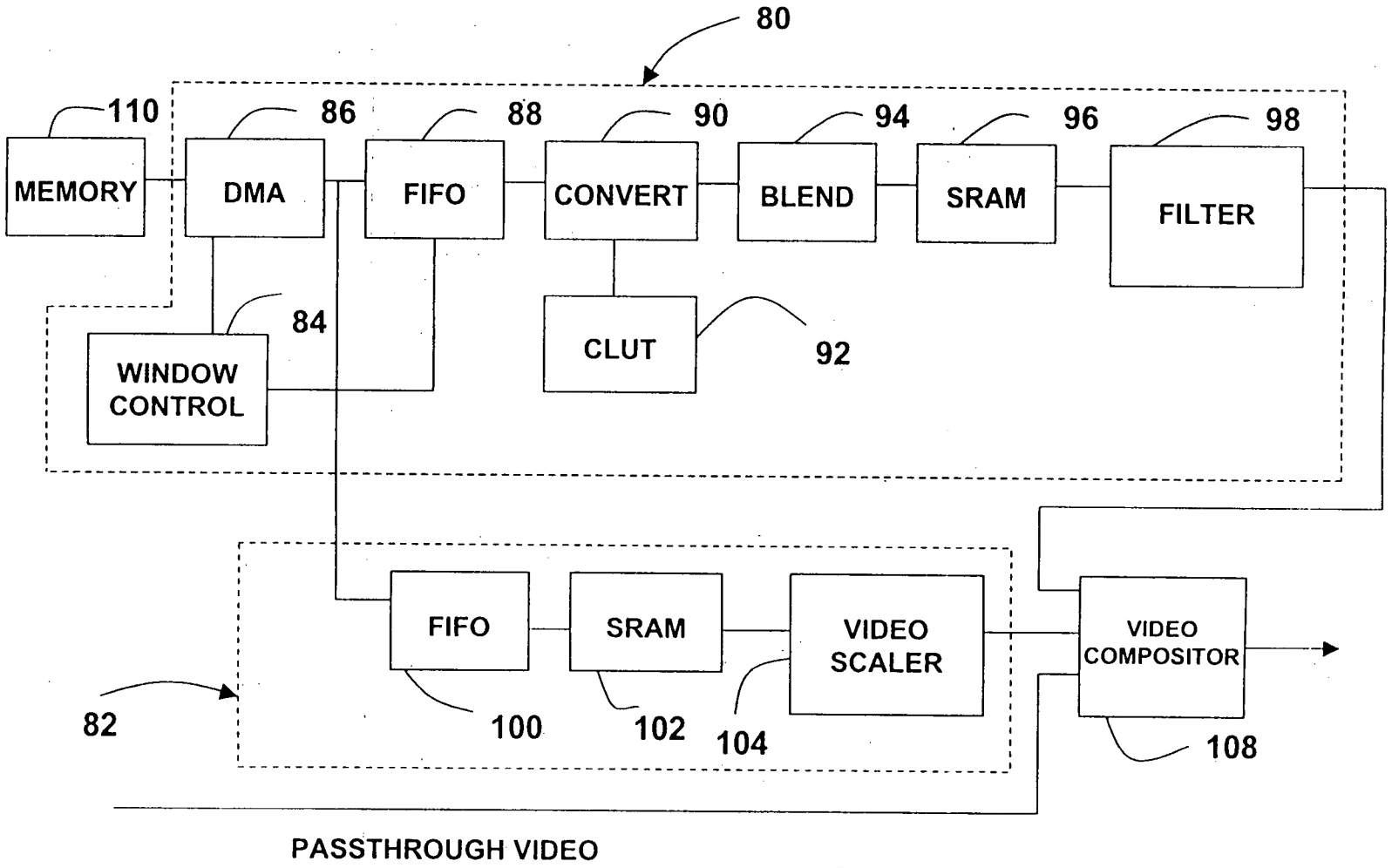

FIG. 4

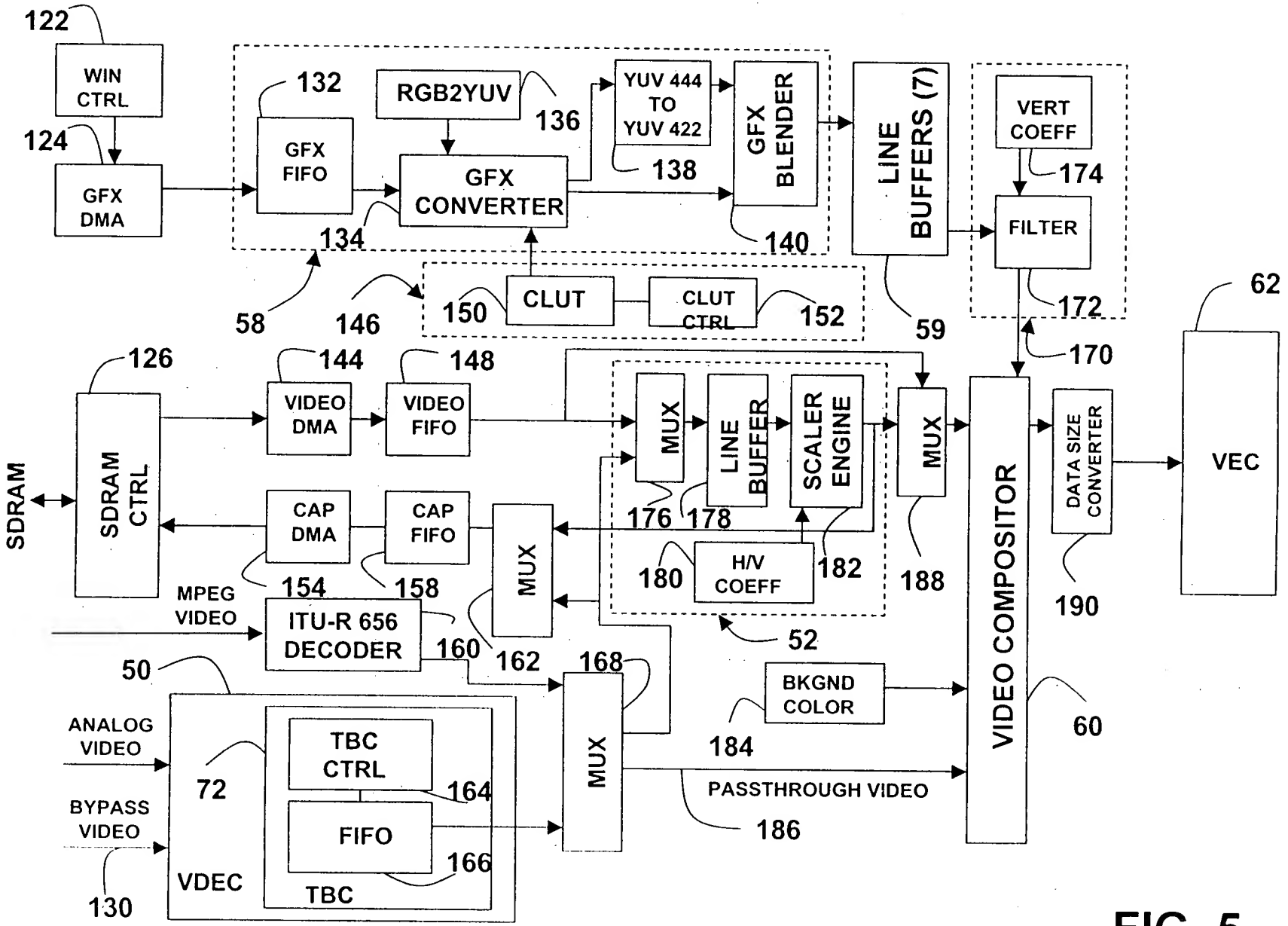

FIG. 5

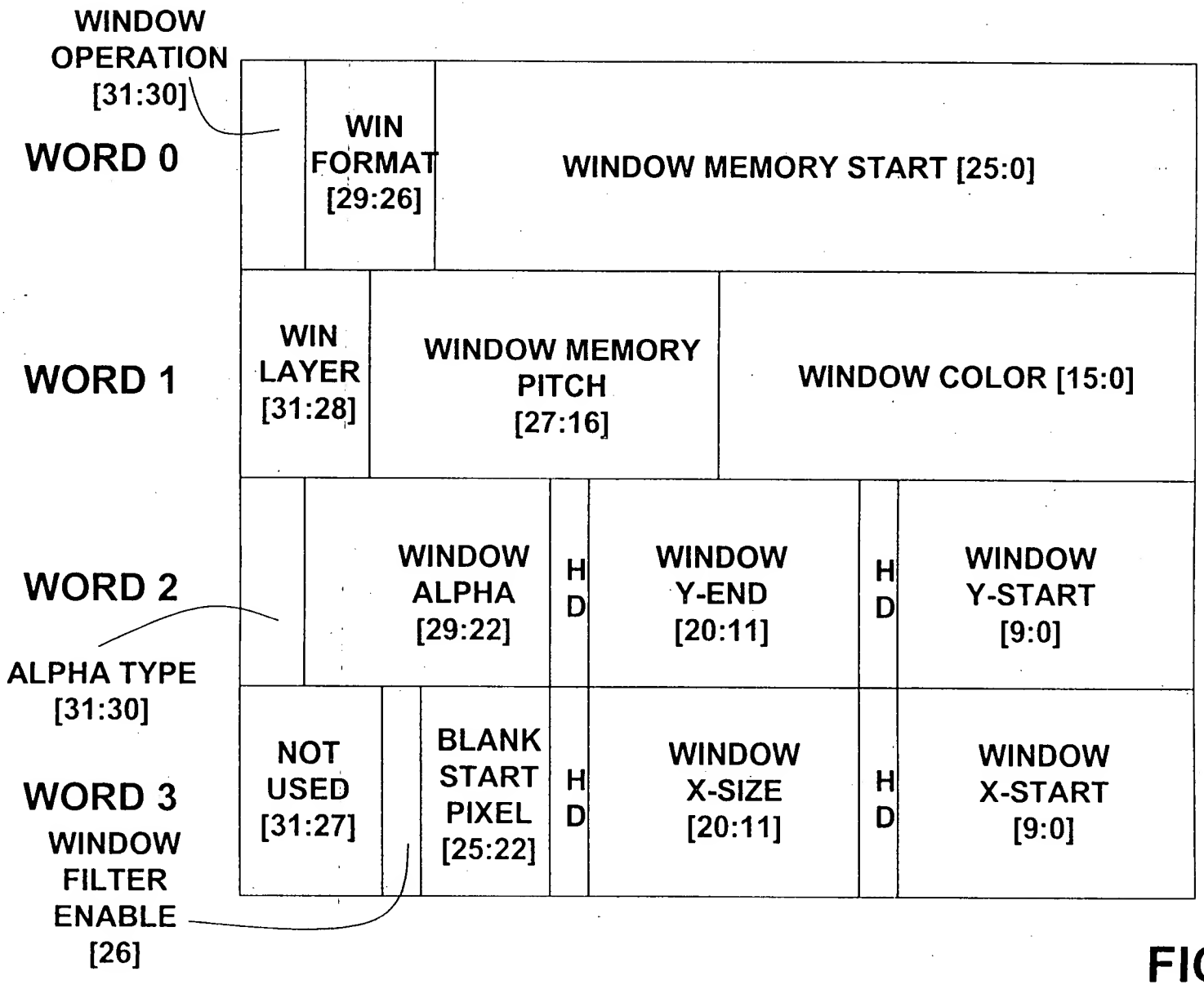

FIG. 6

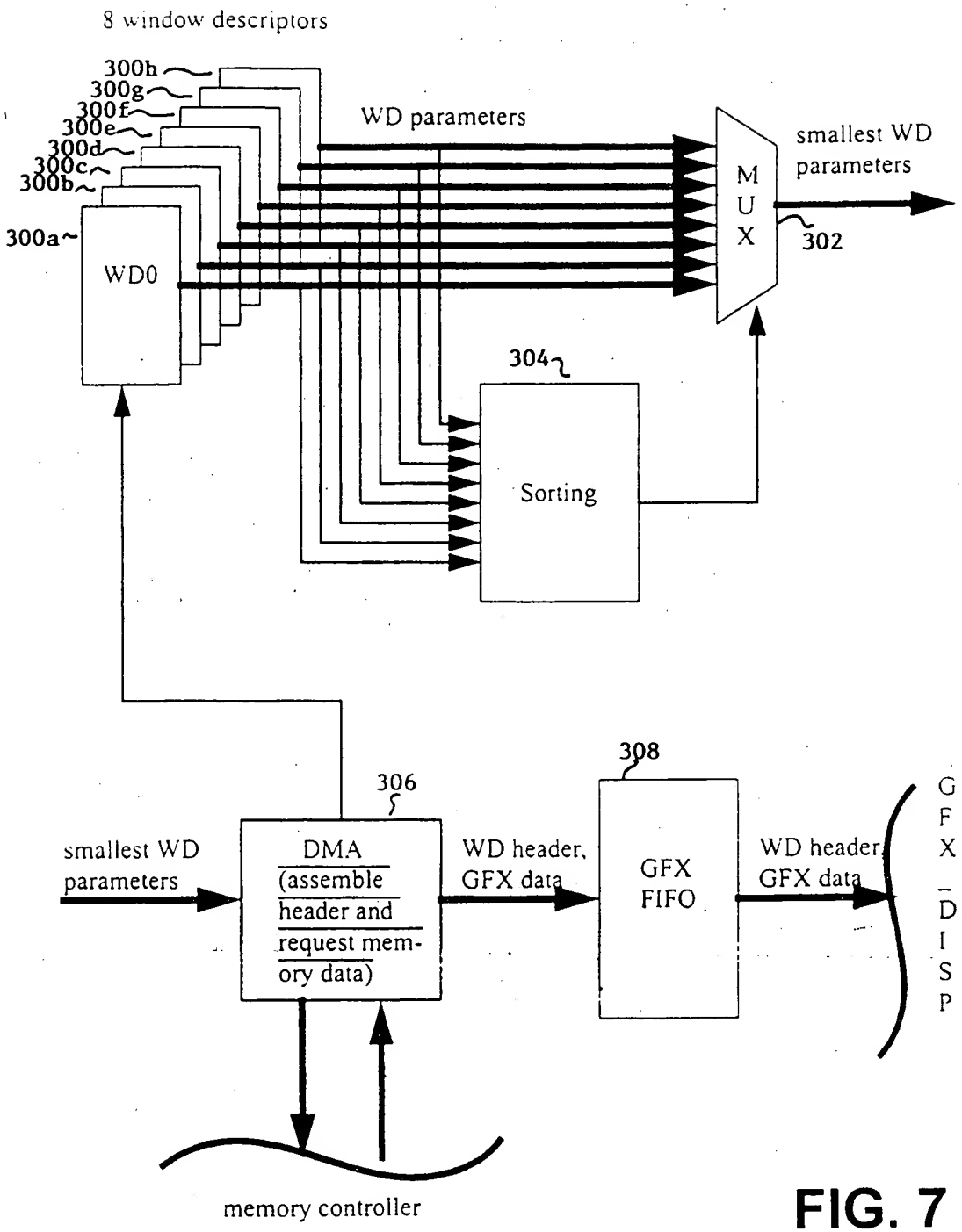
8 window descriptors
300h
300g
300f
300e
300d
300c
300b
300a
WD0
WD parameters
M
U
X
smallest WD parameters
302
304
Sorting
306
DMA (assemble header and request memory data)
smallest WD parameters
WD header, GFX data
308
GFX FIFO
WD header, GFX data
GFX_DISP
memory controller

FIG. 7

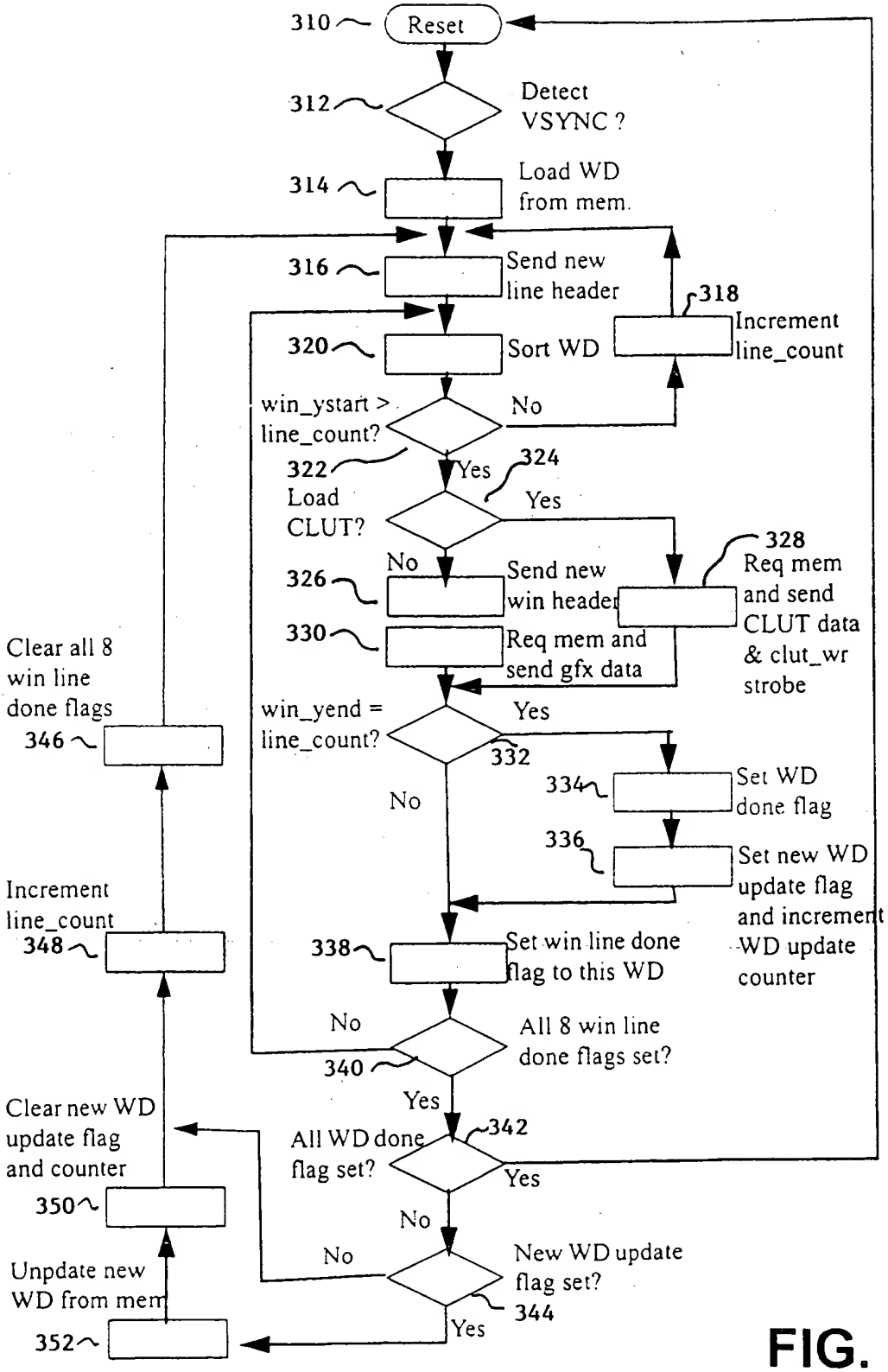
310
Reset
312
Detect VSYNC ?
314
Load WD from mem.
316
Send new line header
318
Increment line_count
320
Sort WD
win_ystart > line_count?
No
322
Load CLUT?
Yes
324
Yes
No
326
Send new win header
328
Req mem and send CLUT data & clut_wr strobe
330
Req mem and send gfx data
win_yend = line_count?
Yes
332
No
334
Set WD done flag
336
Set new WD update flag and increment WD update counter
338
Set win line done flag to this WD
No
340
All 8 win line done flags set?
Yes
342
All WD done flag set?
Yes
No
No
New WD update flag set?
344
Yes
Clear all 8 win line done flags
346
Increment line_count
348
Clear new WD update flag and counter
350
Unpdate new WD from mem
352

FIG. 8

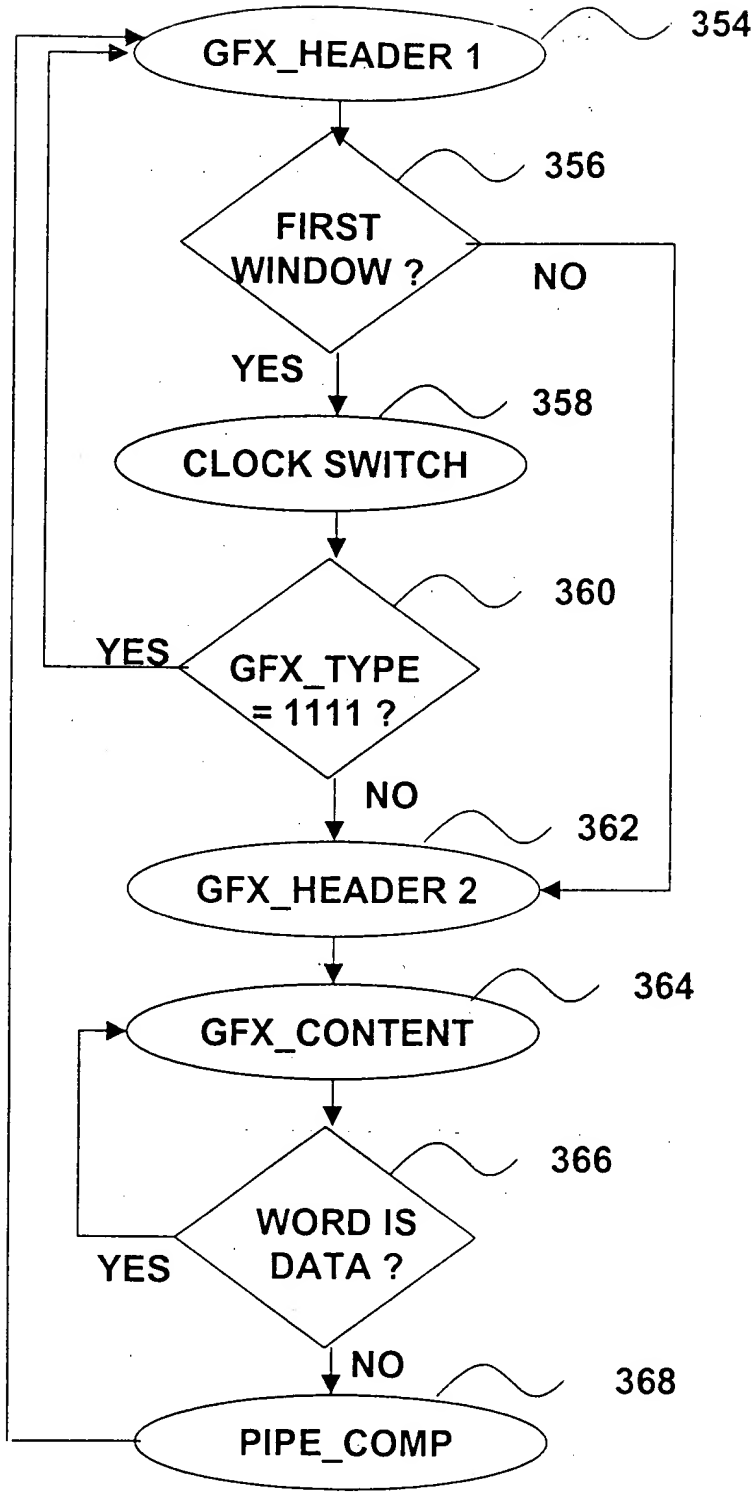
GFX_HEADER 1
354
356
FIRST WINDOW ?
NO
YES
358
CLOCK SWITCH
360
YES
GFX_TYPE = 1111 ?
NO
362
GFX_HEADER 2
364
GFX_CONTENT
366
WORD IS DATA ?
YES
NO
368
PIPE_COMP

FIG. 9

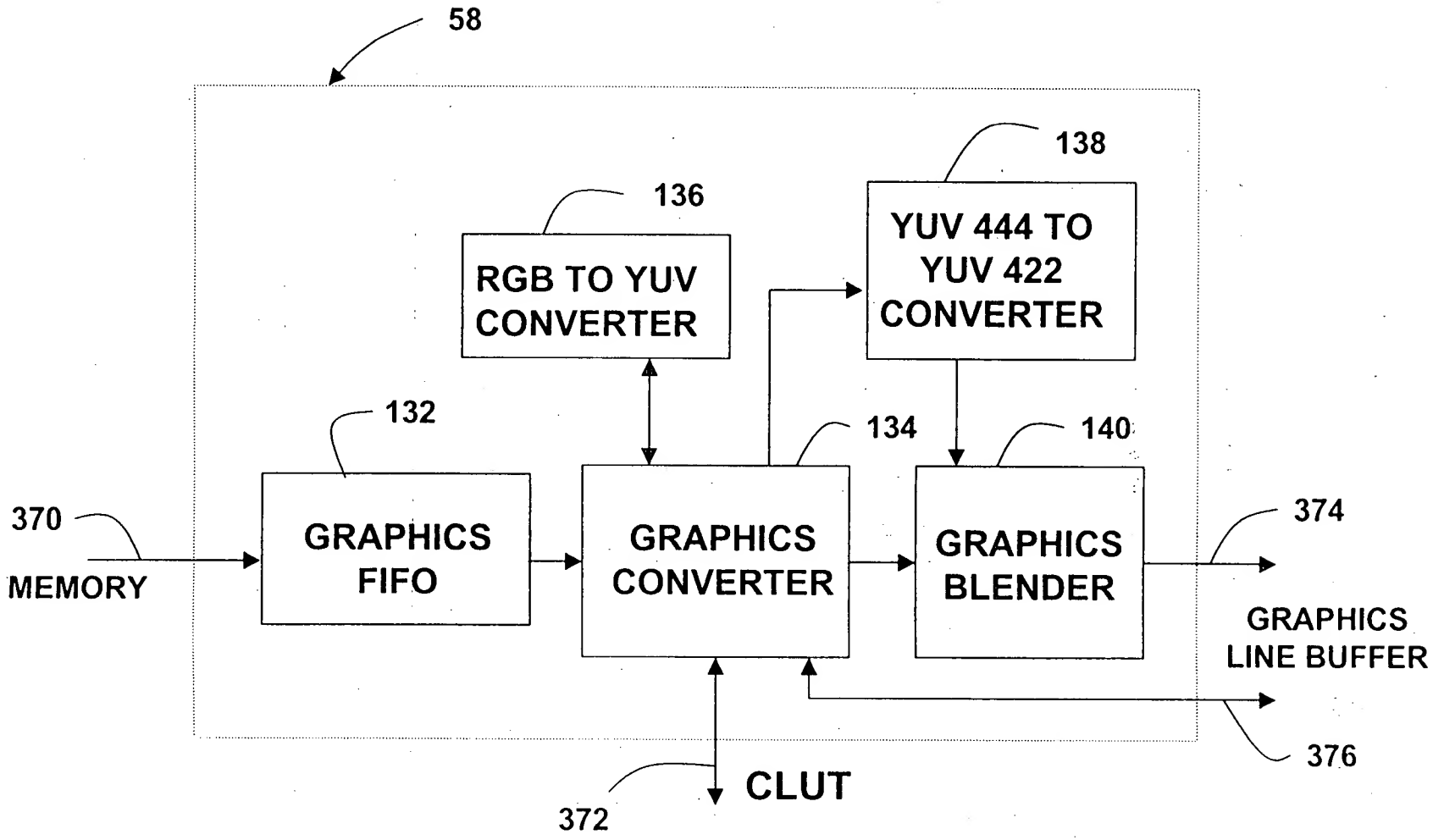
58
138
136
YUV 444 TO
YUV 422
CONVERTER
RGB TO YUV
CONVERTER
132
134
140
370
MEMORY
GRAPHICS
FIFO
GRAPHICS
CONVERTER
GRAPHICS
BLENDER
374
GRAPHICS
LINE BUFFER
376
CLUT
372

FIG. 10

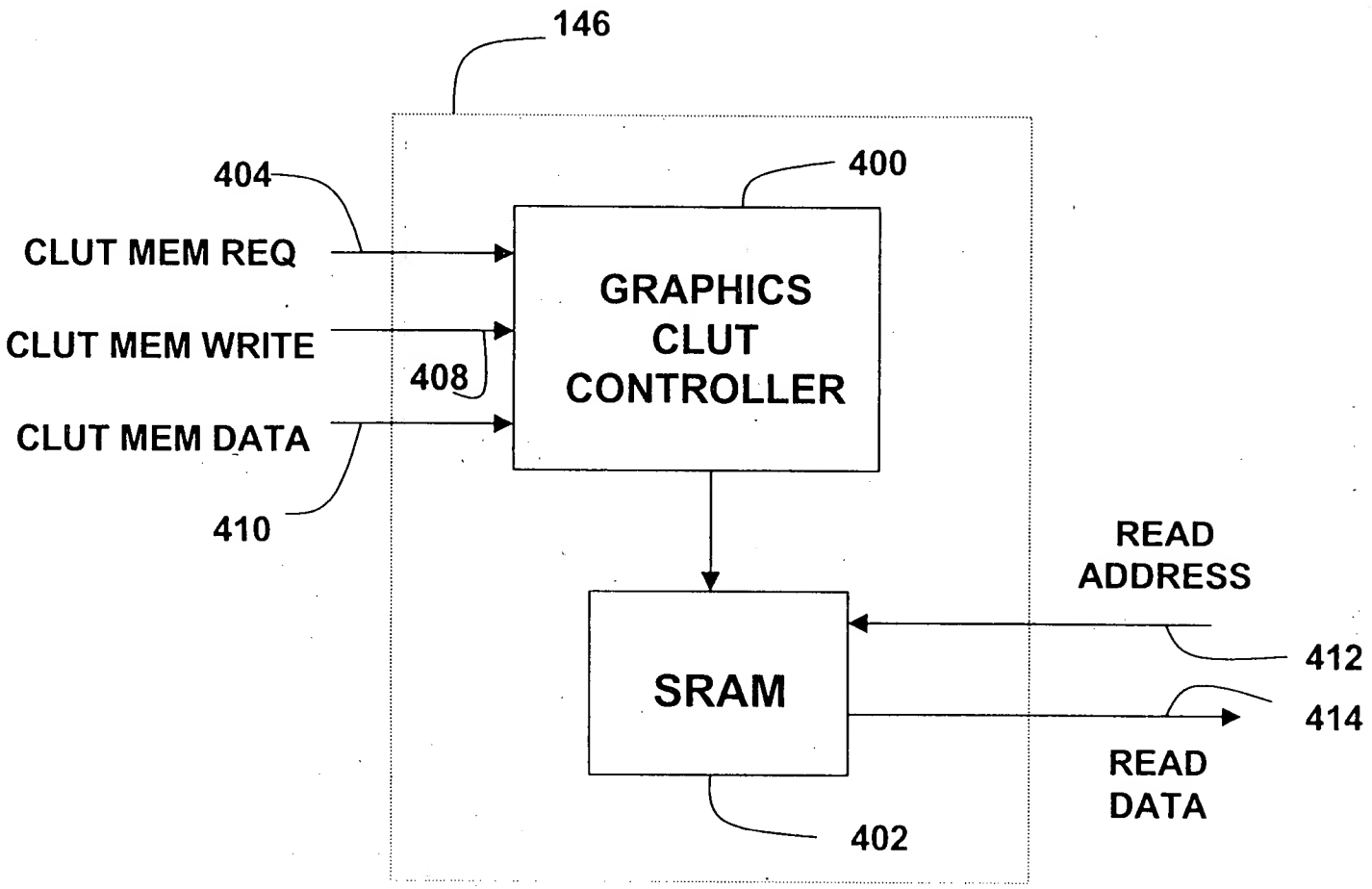
146
404
400
CLUT MEM REQ
CLUT MEM WRITE
408
CLUT MEM DATA
410
GRAPHICS CLUT CONTROLLER
READ ADDRESS
412
SRAM
414
READ DATA
402

FIG. 11

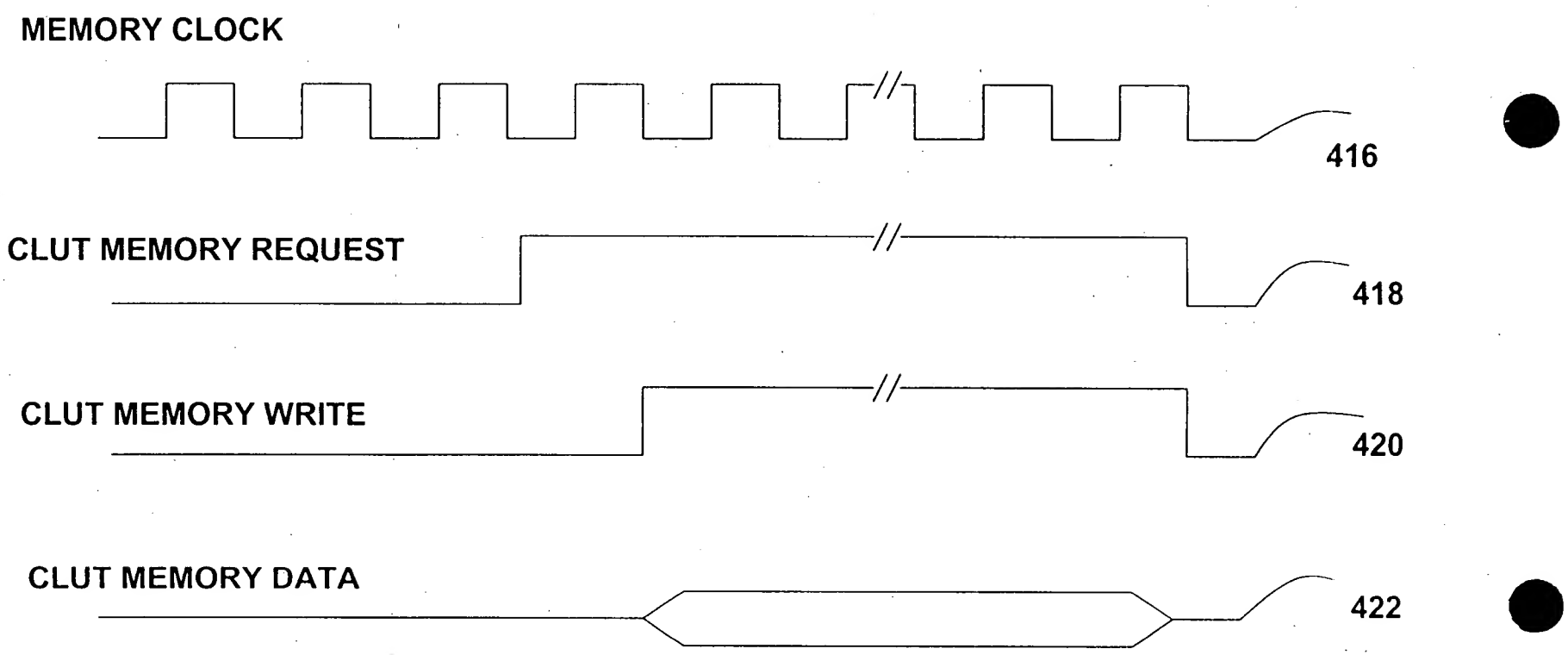
MEMORY CLOCK
416
CLUT MEMORY REQUEST
418
CLUT MEMORY WRITE
420
CLUT MEMORY DATA
422

FIG. 12

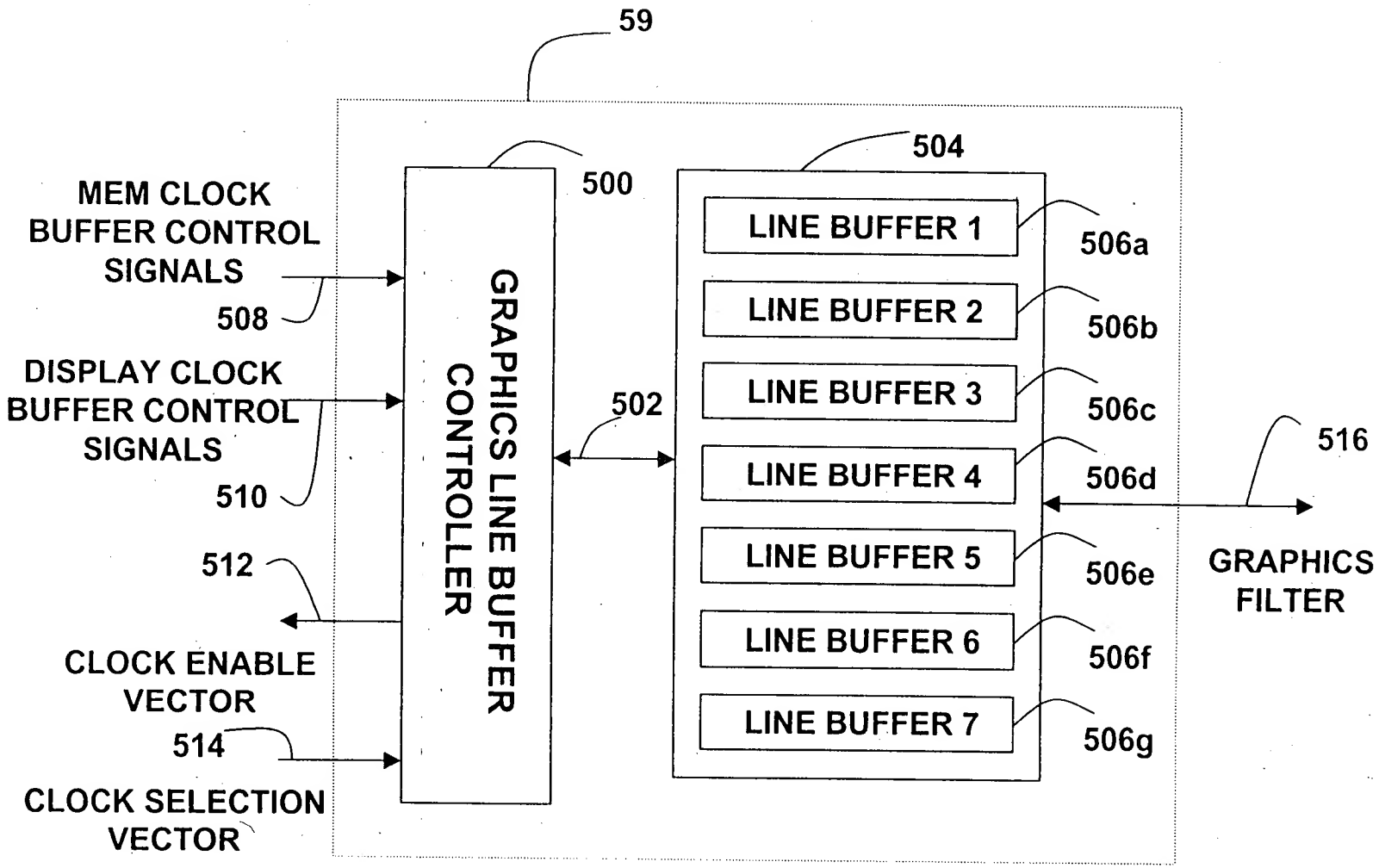
59
500
504
MEM CLOCK BUFFER CONTROL SIGNALS
508
DISPLAY CLOCK BUFFER CONTROL SIGNALS
510
512
CLOCK ENABLE VECTOR
514
CLOCK SELECTION VECTOR
GRAPHICS LINE BUFFER CONTROLLER
502
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
LINE BUFFER 6
LINE BUFFER 7
506a
506b
506c
506d
506e
506f
506g
516
GRAPHICS FILTER

FIG. 13

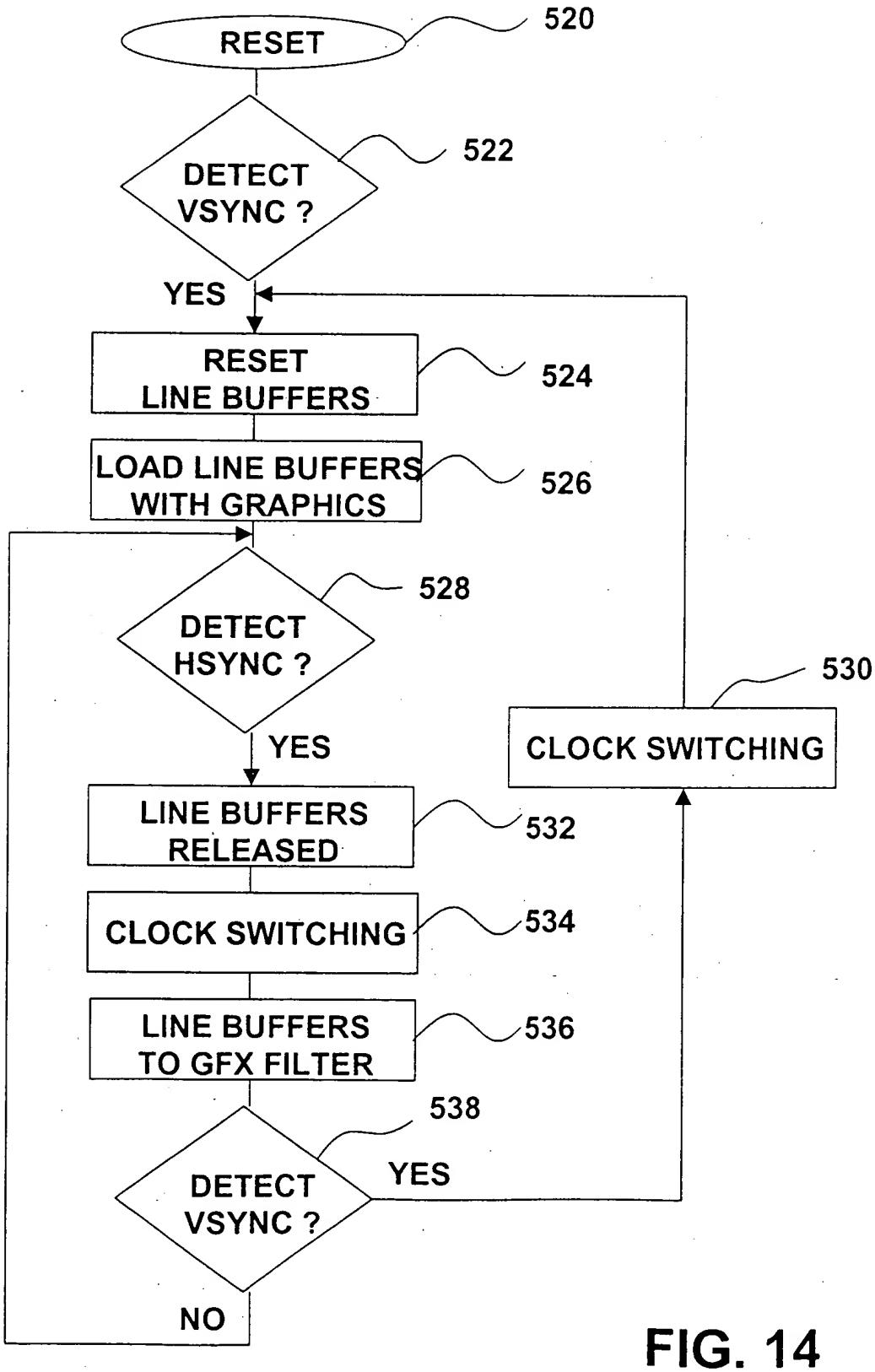
RESET
520
DETECT VSYNC ?
522
YES
RESET LINE BUFFERS
524
LOAD LINE BUFFERS WITH GRAPHICS
526
DETECT HSYNC ?
528
YES
LINE BUFFERS RELEASED
532
CLOCK SWITCHING
534
LINE BUFFERS TO GFX FILTER
536
DETECT VSYNC ?
538
YES
NO
CLOCK SWITCHING
530

FIG. 14

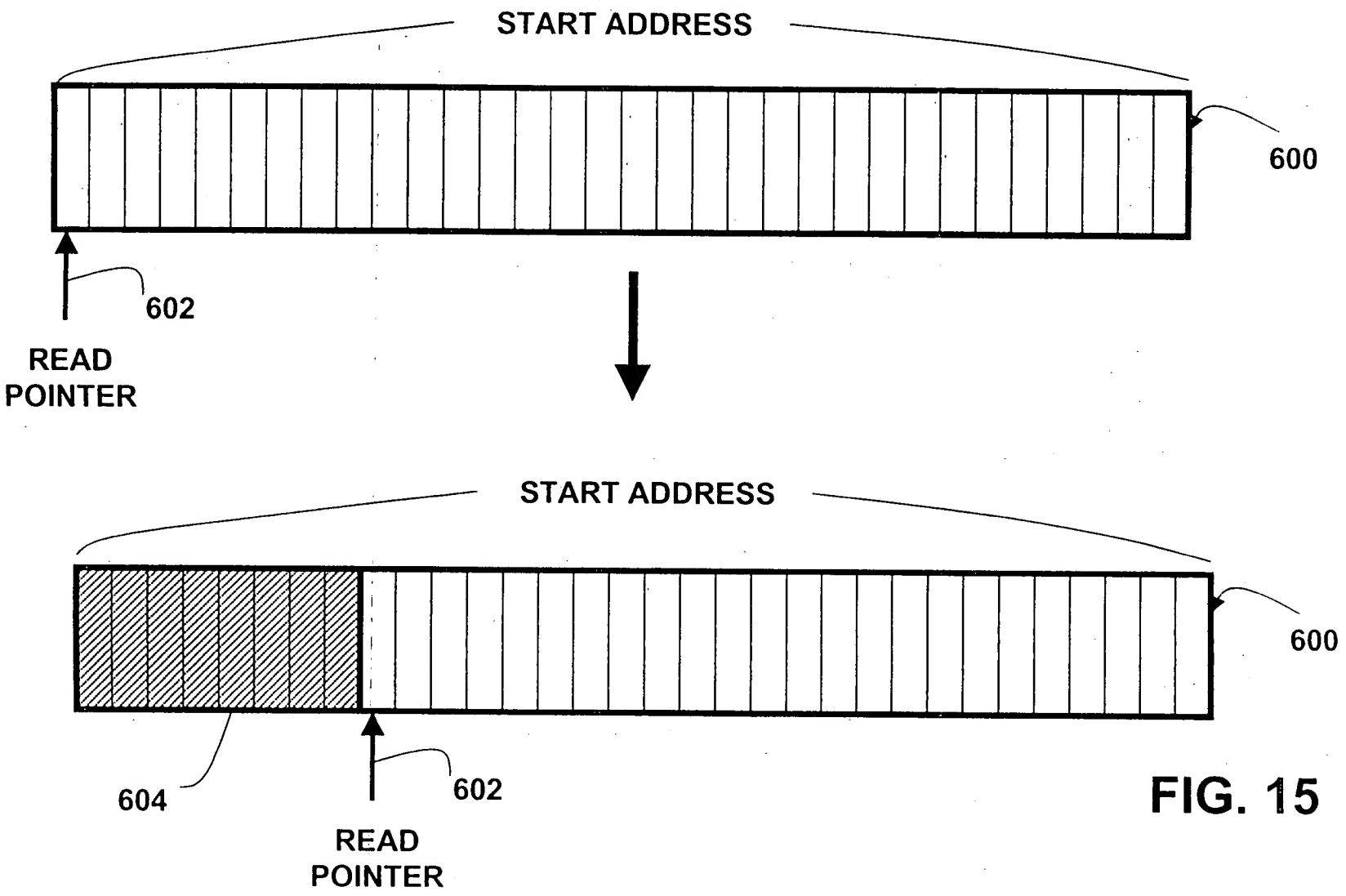
START ADDRESS
600
602
READ POINTER
START ADDRESS
600
604
602
READ POINTER

FIG. 15

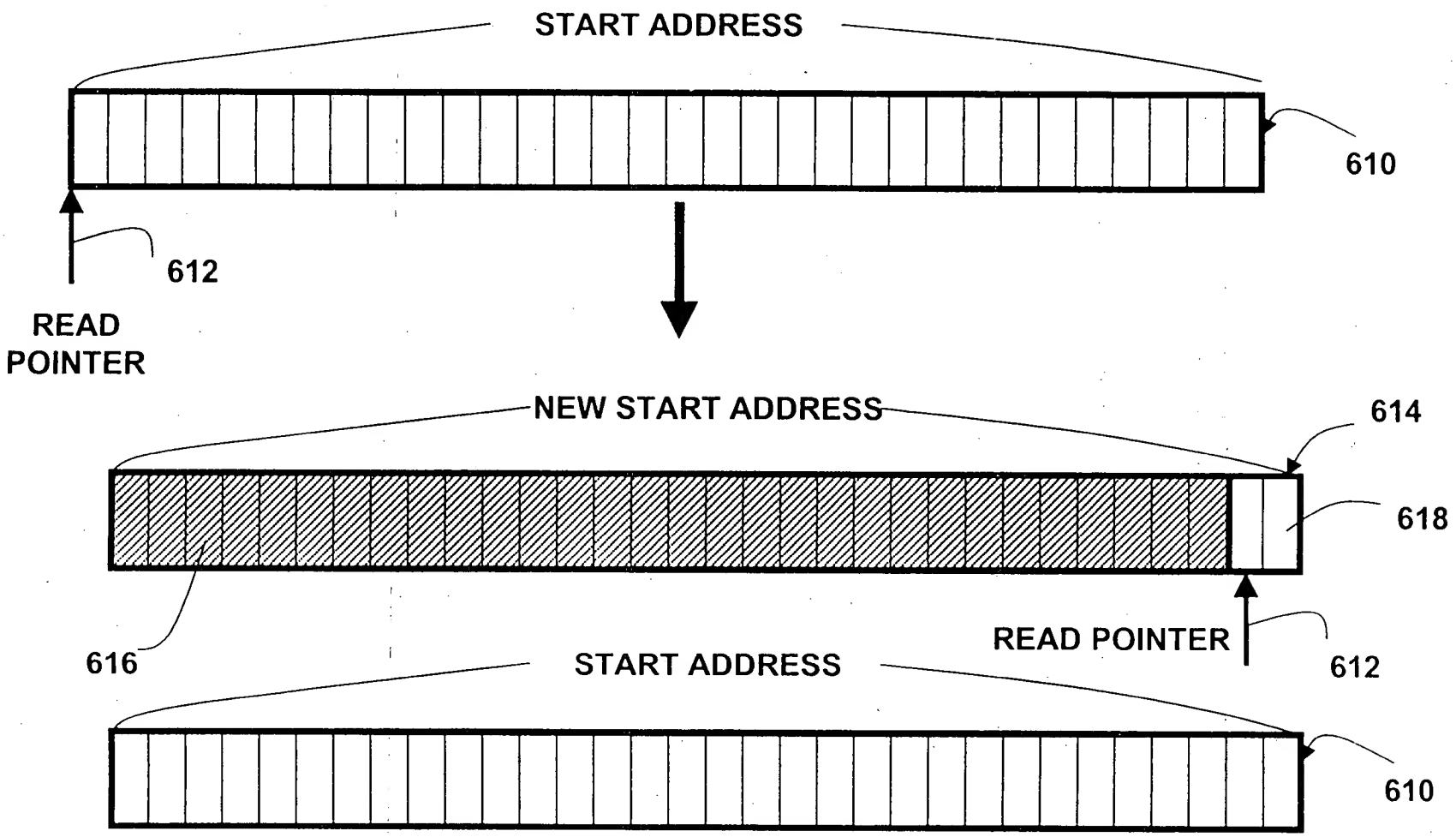
START ADDRESS
610
612
READ POINTER
NEW START ADDRESS
614
618
616
READ POINTER
612
START ADDRESS
610

FIG. 16

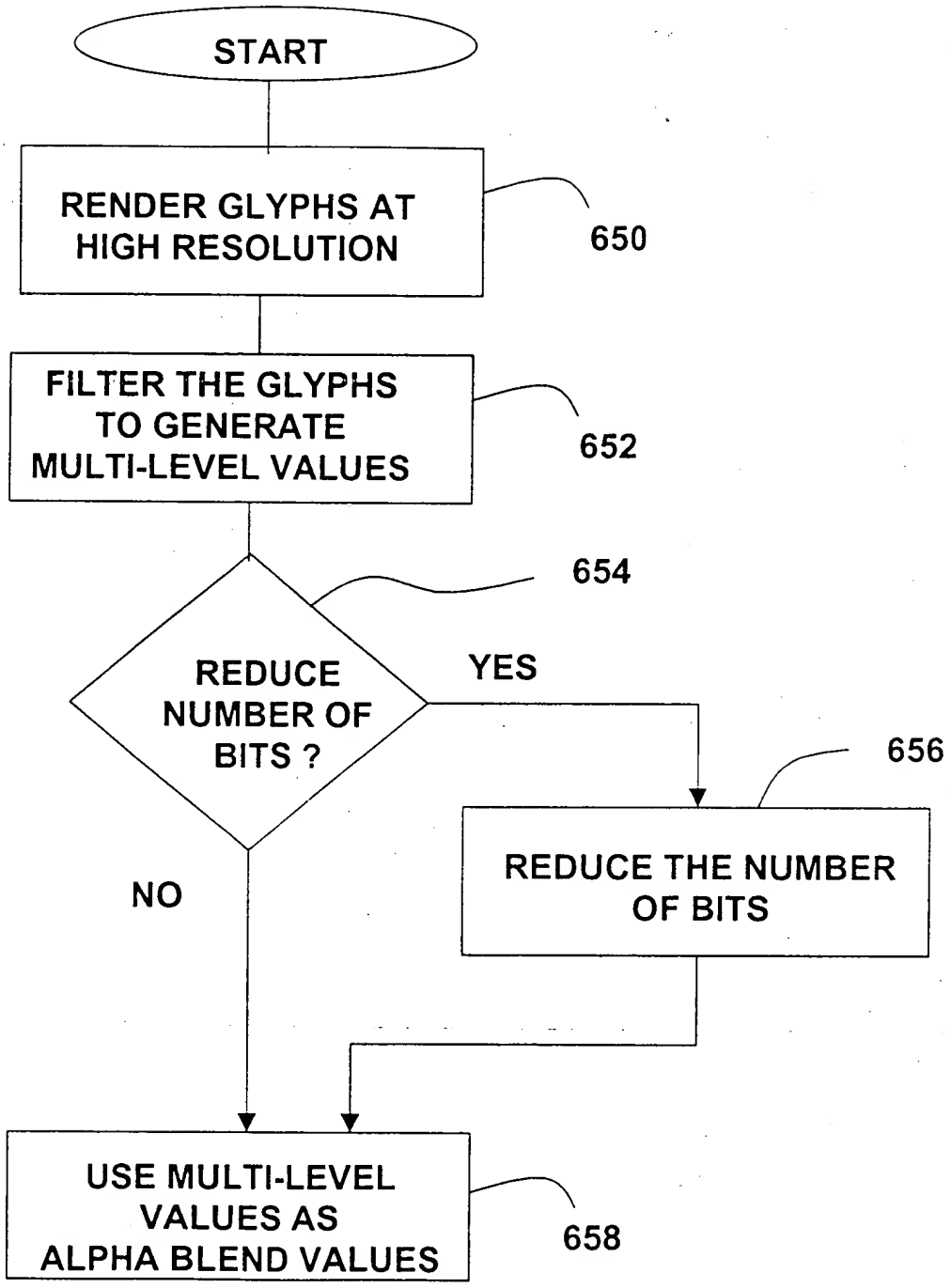
START
RENDER GLYPHS AT HIGH RESOLUTION
650
FILTER THE GLYPHS TO GENERATE MULTI-LEVEL VALUES
652
654
REDUCE NUMBER OF BITS ?
YES
NO
656
REDUCE THE NUMBER OF BITS
USE MULTI-LEVEL VALUES AS ALPHA BLEND VALUES
658

FIG. 17

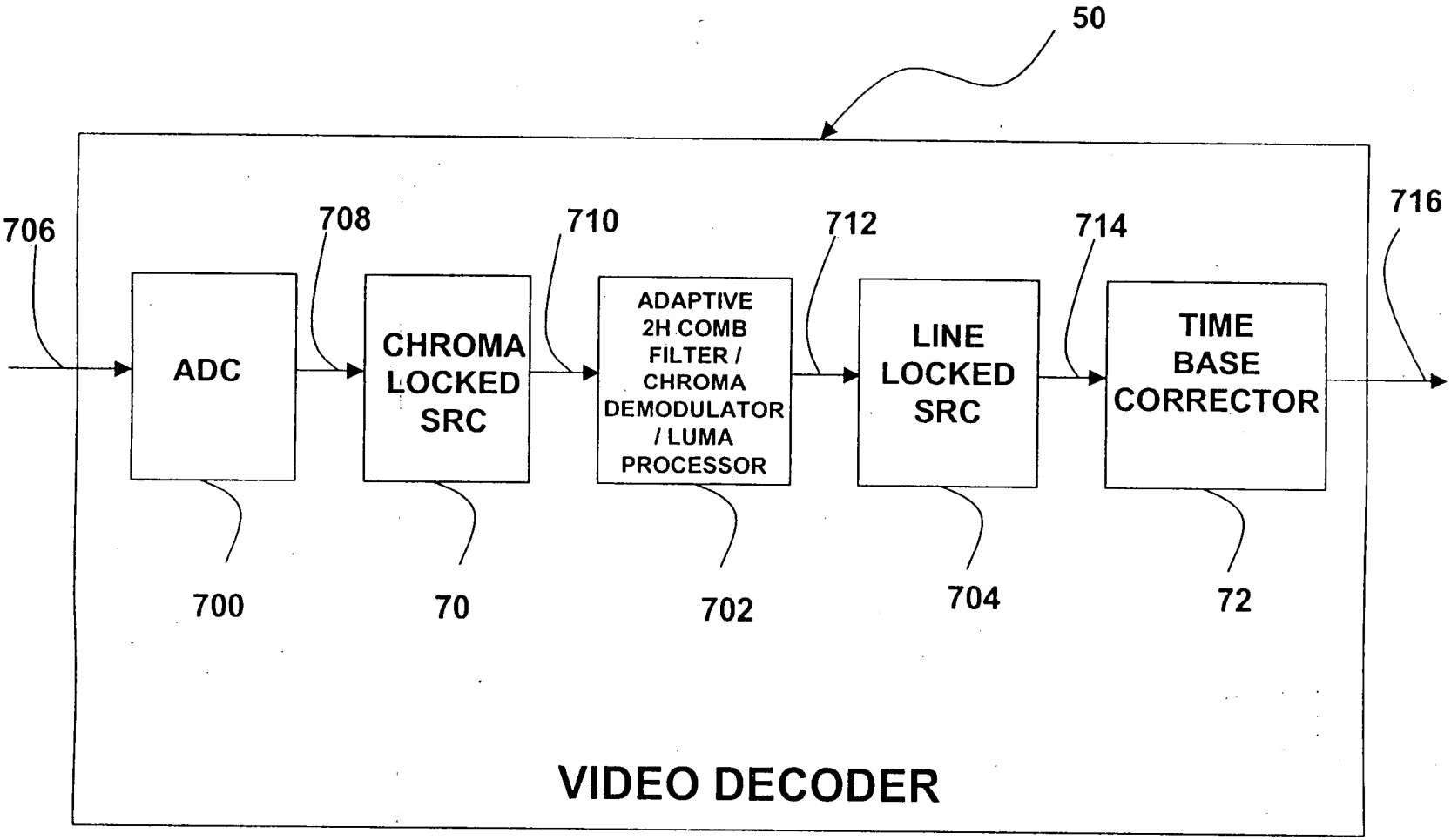
50
706
708
710
712
714
716
ADC
CHROMA LOCKED SRC
ADAPTIVE 2H COMB FILTER / CHROMA DEMODULATOR / LUMA PROCESSOR
LINE LOCKED SRC
TIME BASE CORRECTOR
700
70
702
704
72
VIDEO DECODER

FIG. 18

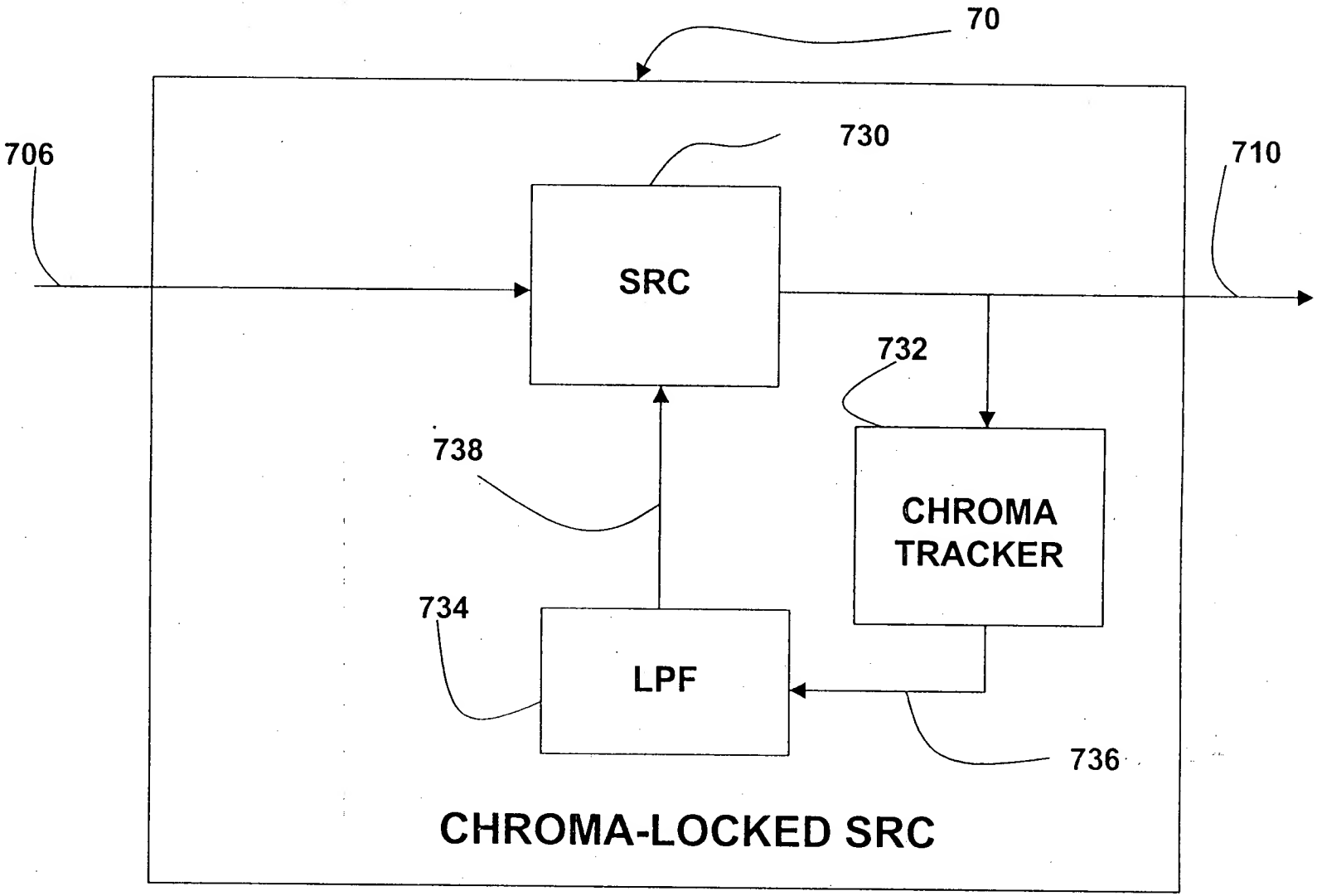

FIG. 19

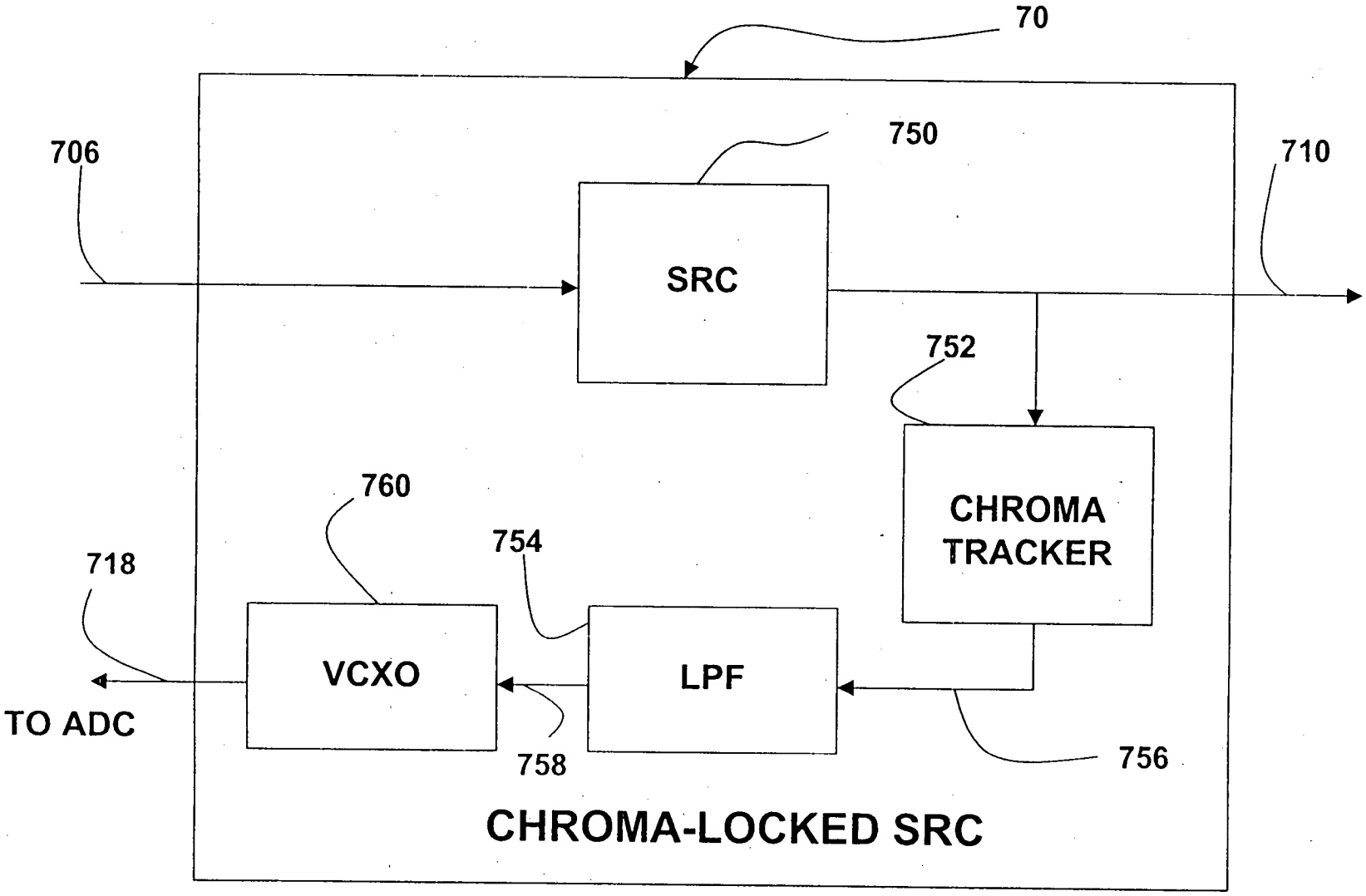

FIG. 20

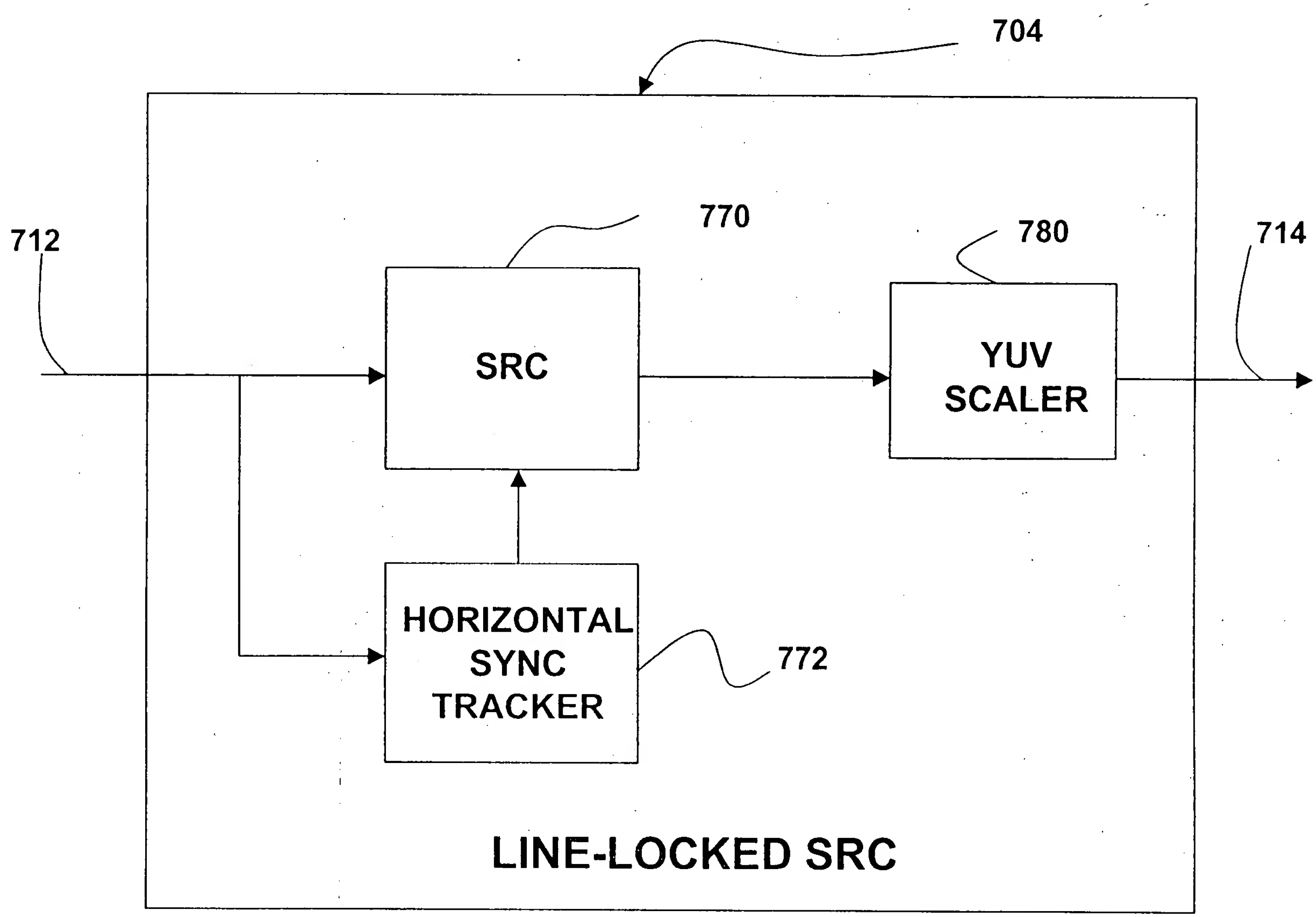
704
770
780
712
714
SRC
YUV
SCALER
HORIZONTAL
SYNC
TRACKER
772
LINE-LOCKED SRC

FIG. 21

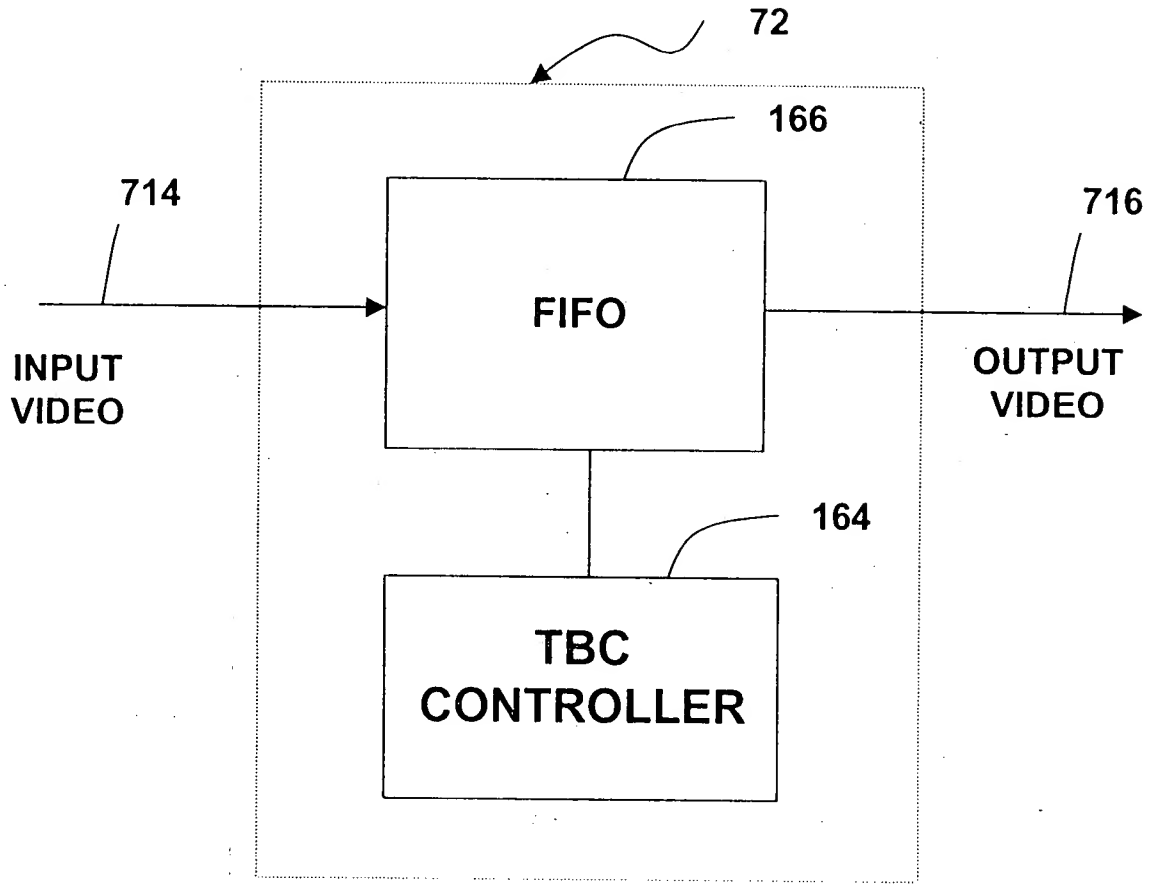
72
166
714
716
FIFO
INPUT
VIDEO
OUTPUT
VIDEO
164
TBC
CONTROLLER

FIG. 22

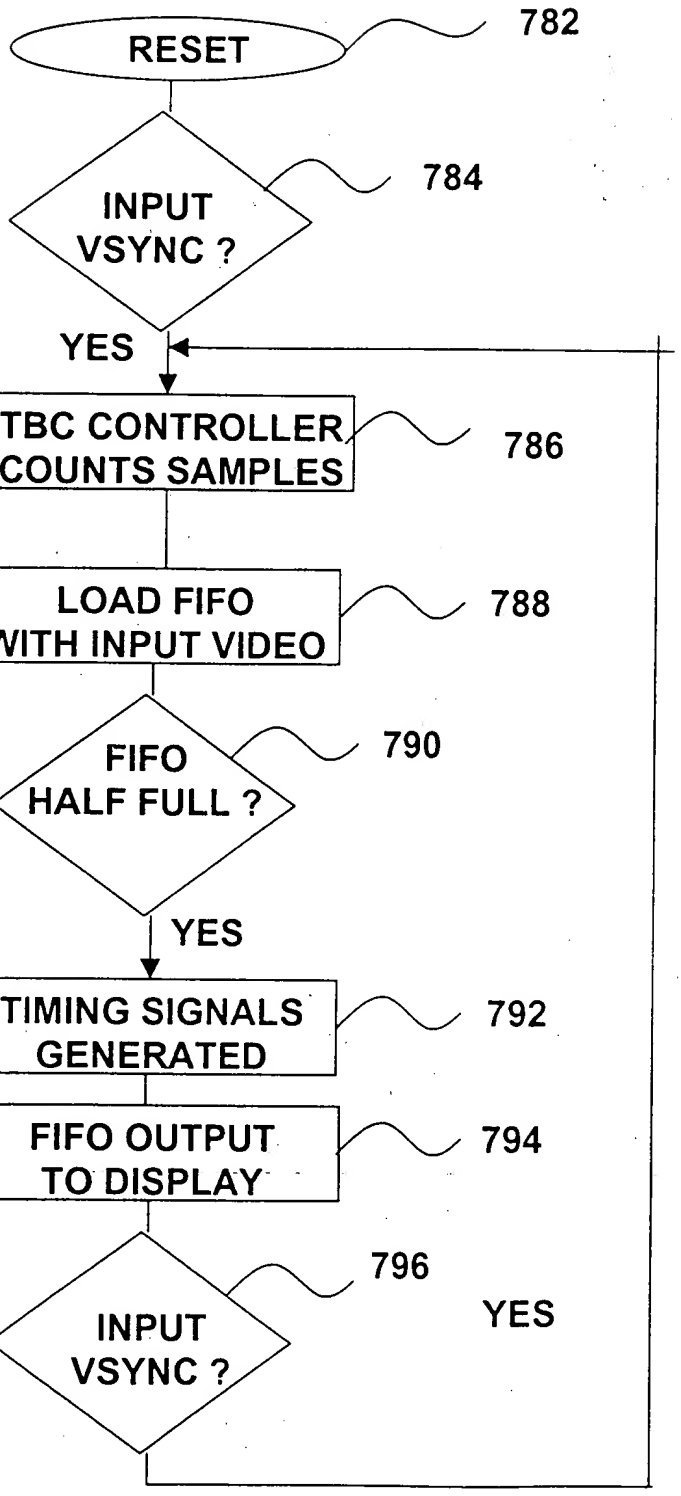
RESET
782
INPUT VSYNC ?
784
YES
TBC CONTROLLER COUNTS SAMPLES
786
LOAD FIFO WITH INPUT VIDEO
788
FIFO HALF FULL ?
790
YES
TIMING SIGNALS GENERATED
792
FIFO OUTPUT TO DISPLAY
794
INPUT VSYNC ?
796
YES

FIG. 23

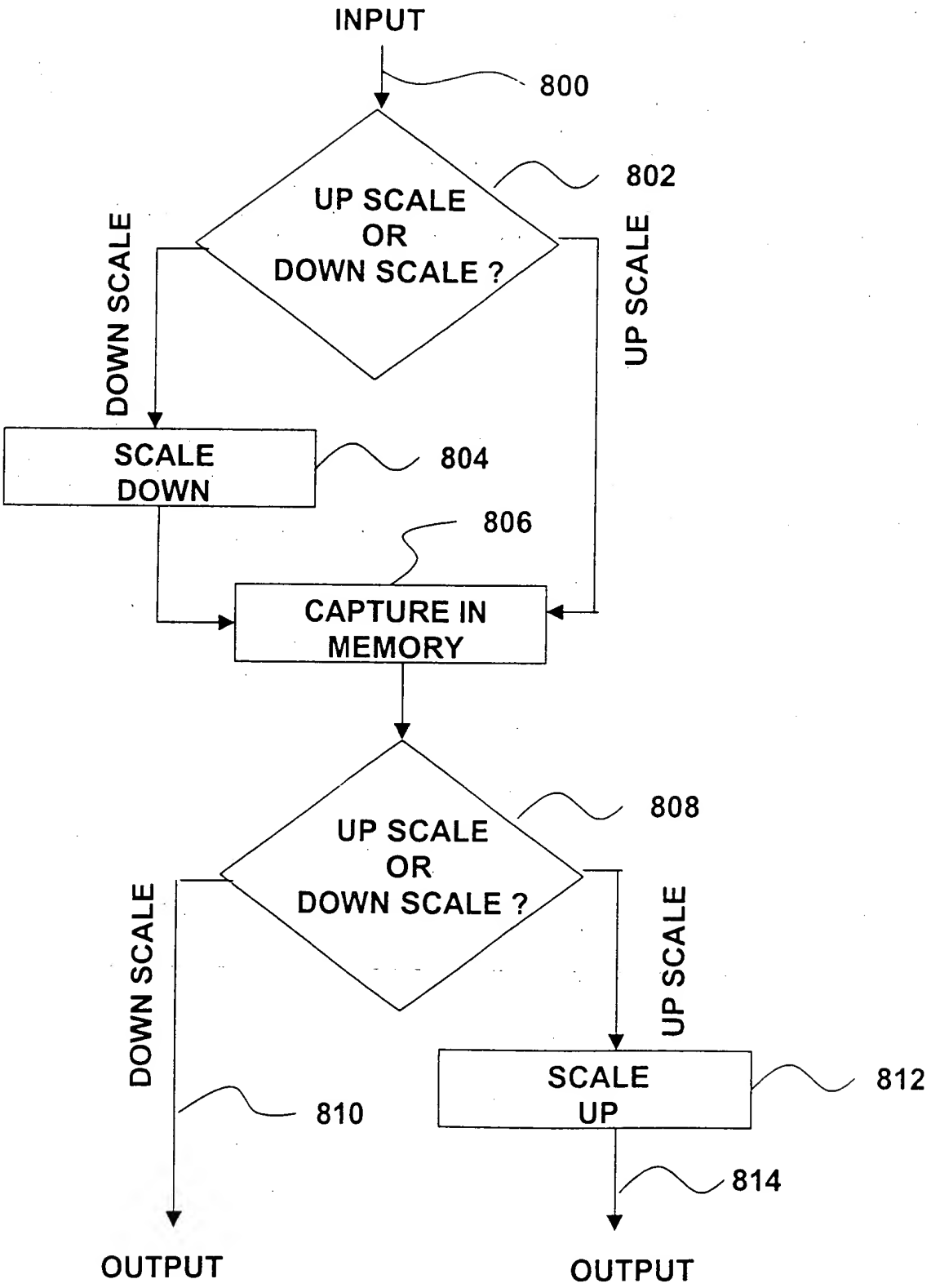
INPUT
800
UP SCALE OR DOWN SCALE ?
802
DOWN SCALE
UP SCALE
SCALE DOWN
804
806
CAPTURE IN MEMORY
UP SCALE OR DOWN SCALE ?
808
DOWN SCALE
UP SCALE
SCALE UP
812
810
814
OUTPUT
OUTPUT

FIG. 24

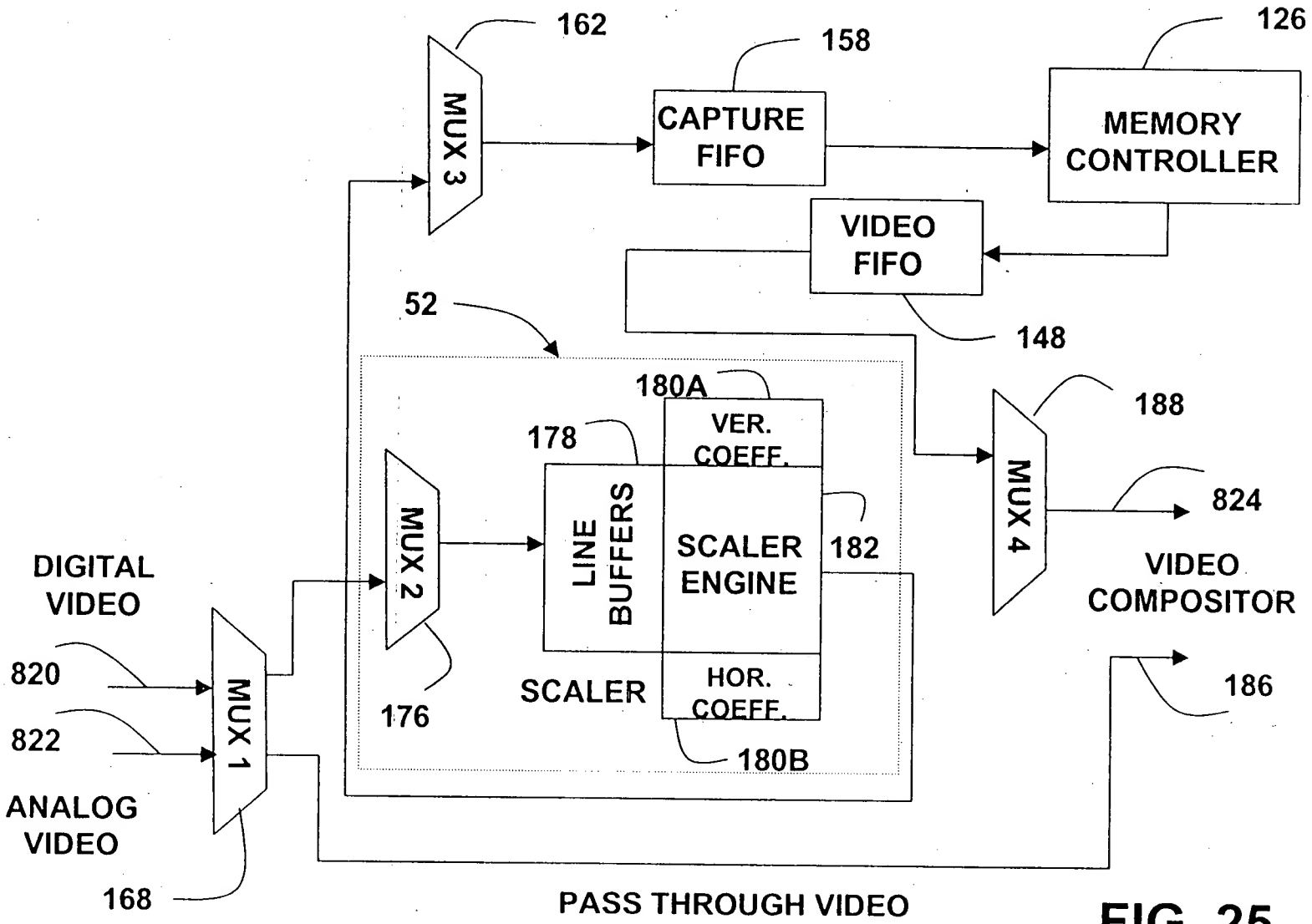

FIG. 25

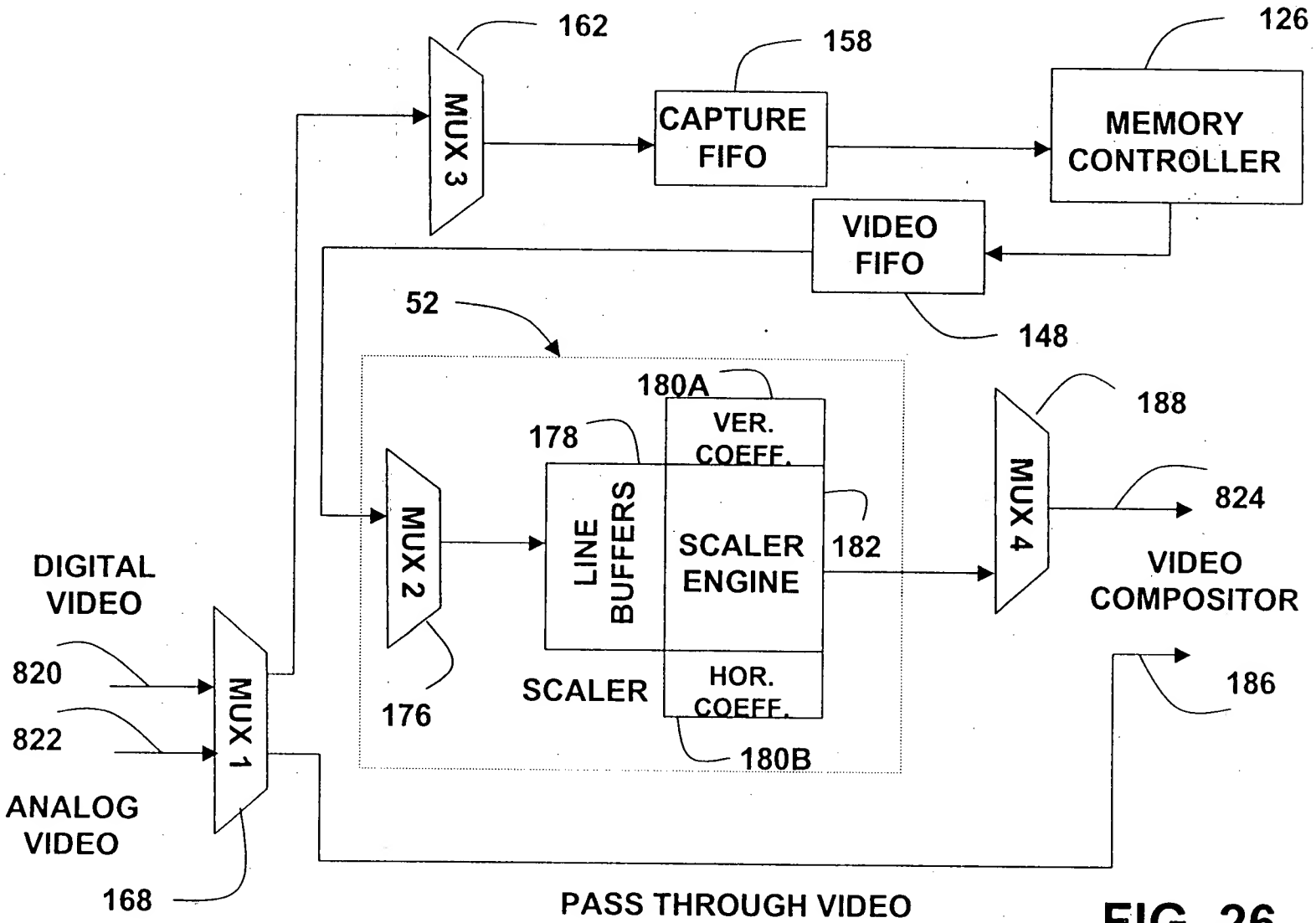

FIG. 26

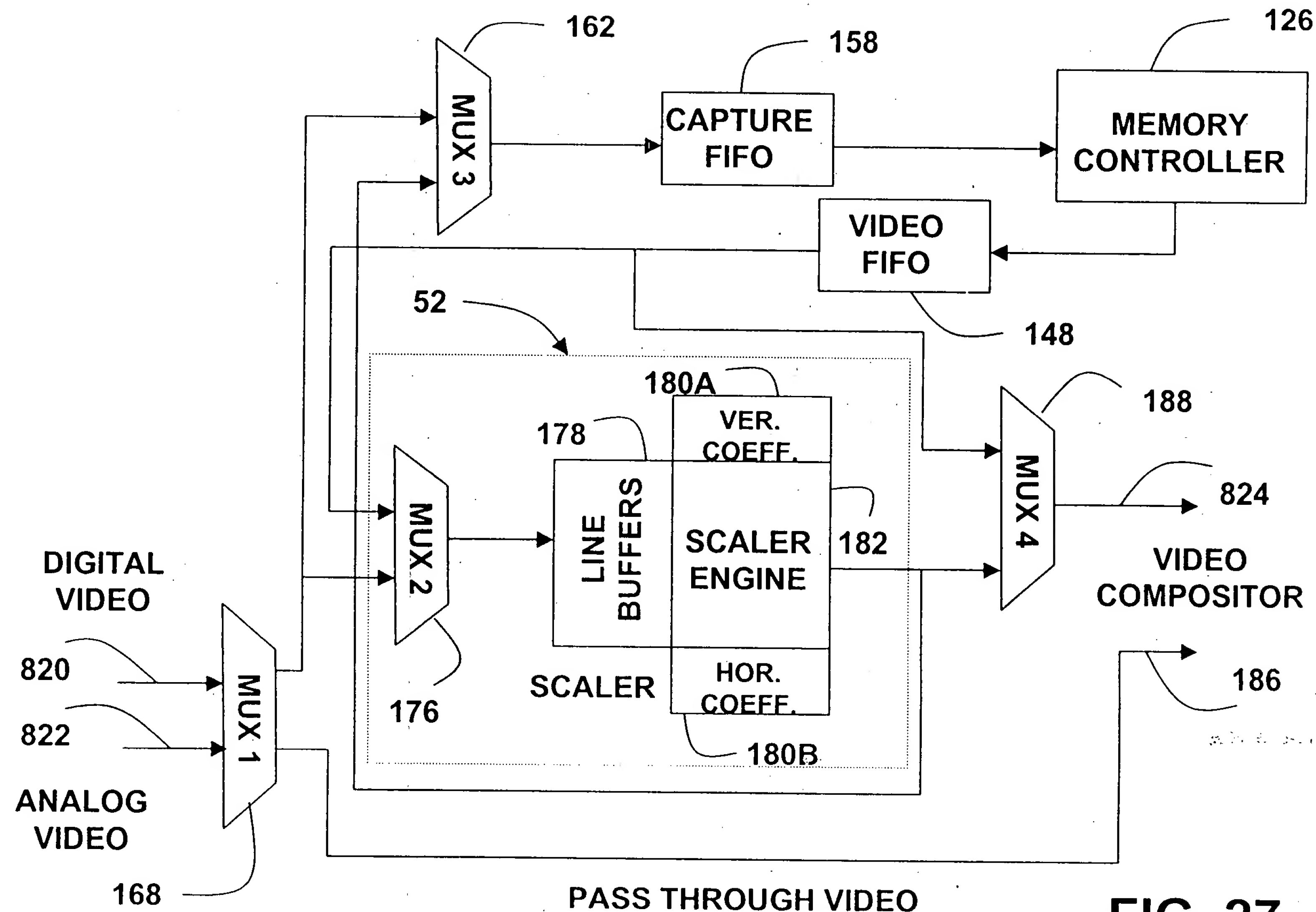
162
MUX 3
158
CAPTURE FIFO
126
MEMORY CONTROLLER
VIDEO FIFO
148
52
180A
VER. COEFF.
178
LINE BUFFERS
SCALER ENGINE
182
MUX 2
176
SCALER
HOR. COEFF.
180B
188
MUX 4
824
VIDEO COMPOSITOR
186
DIGITAL VIDEO
820
822
ANALOG VIDEO
MUX 1
168
PASS THROUGH VIDEO

FIG. 27

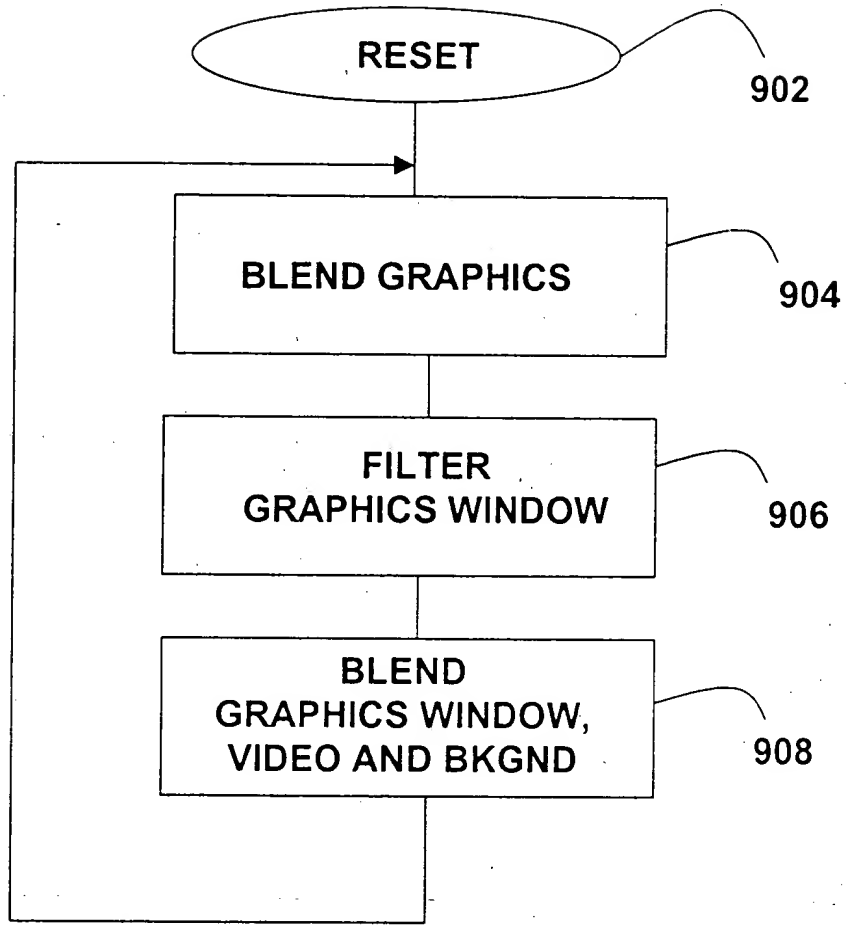
RESET
902
BLEND GRAPHICS
904
FILTER
GRAPHICS WINDOW
906
BLEND
GRAPHICS WINDOW,
VIDEO AND BKGND
908

FIG. 28

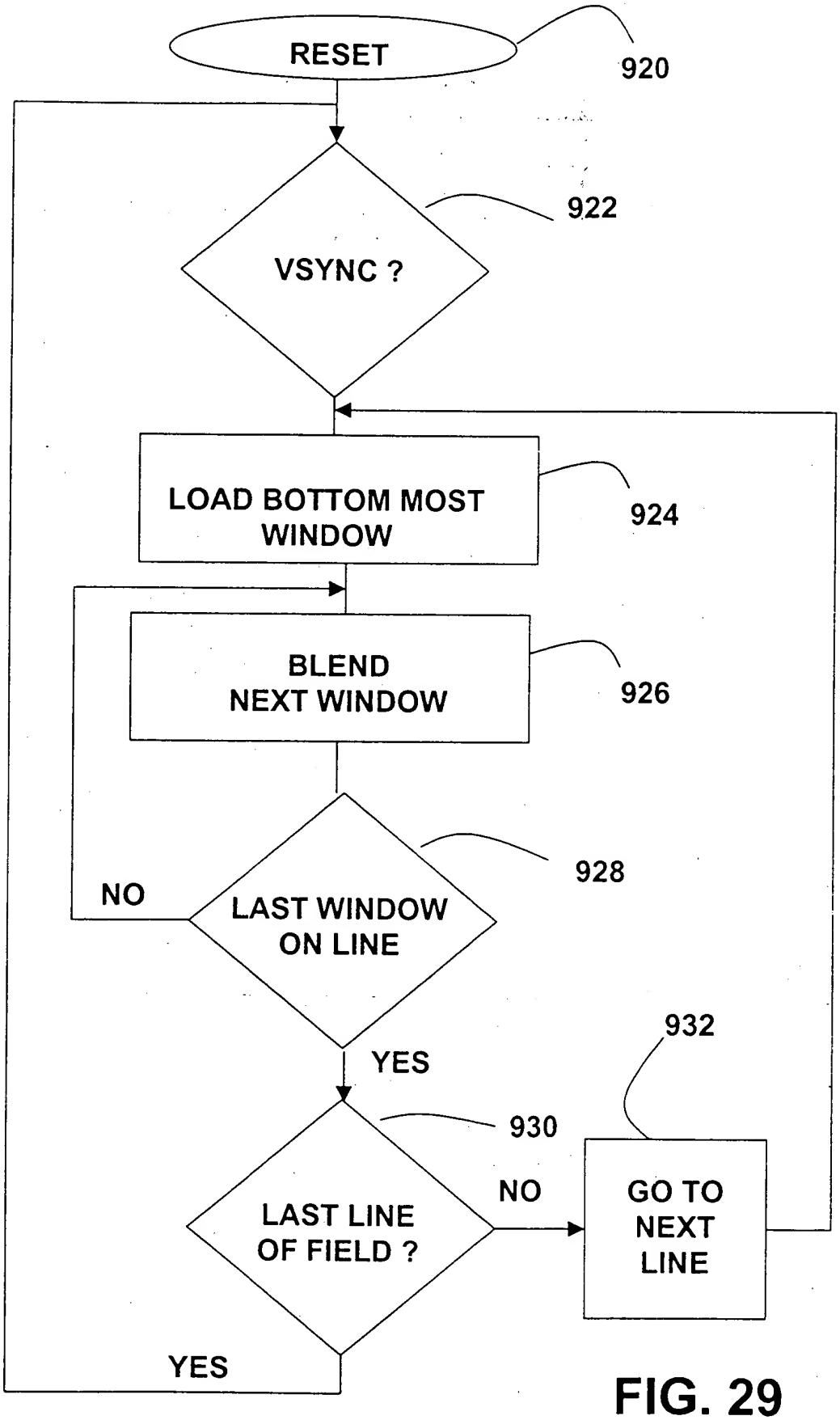
RESET
920
VSYNC ?
922
LOAD BOTTOM MOST WINDOW
924
BLEND NEXT WINDOW
926
LAST WINDOW ON LINE
928
NO
YES
LAST LINE OF FIELD ?
930
NO
GO TO NEXT LINE
932
YES

FIG. 29

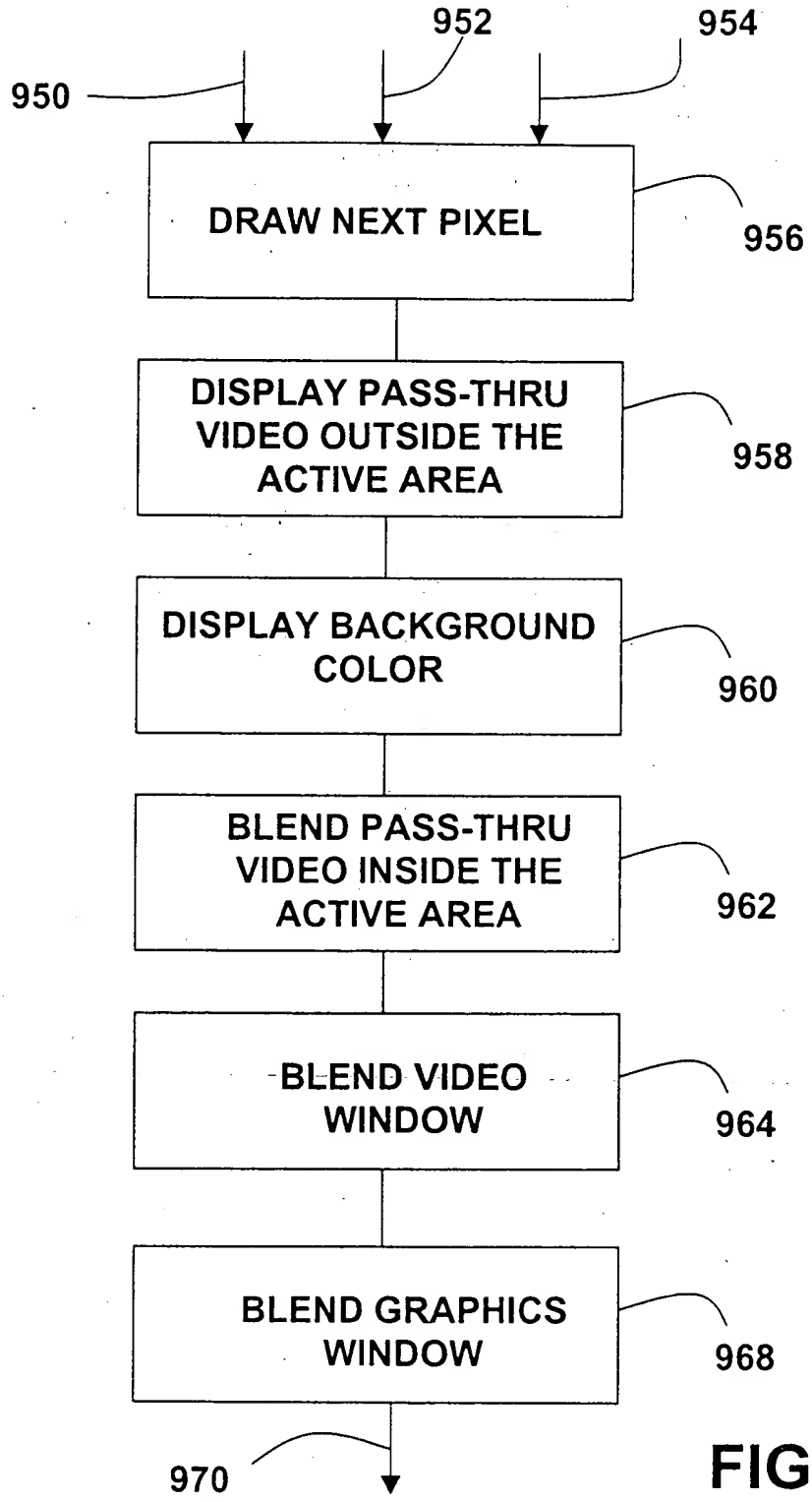
950
952
954
DRAW NEXT PIXEL
956
DISPLAY PASS-THRU VIDEO OUTSIDE THE ACTIVE AREA
958
DISPLAY BACKGROUND COLOR
960
BLEND PASS-THRU VIDEO INSIDE THE ACTIVE AREA
962
BLEND VIDEO WINDOW
964
BLEND GRAPHICS WINDOW
968
970

FIG. 30

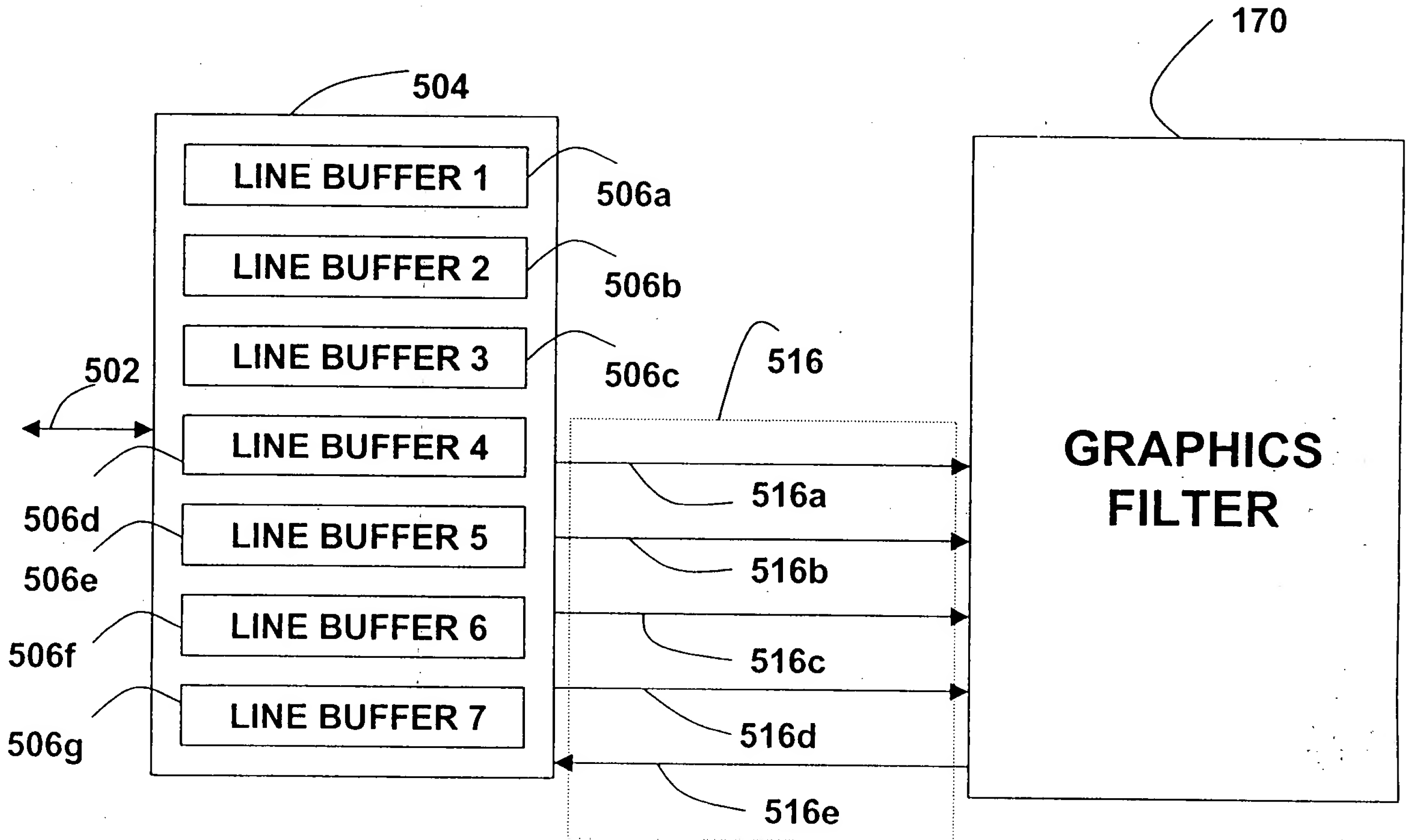
504
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
LINE BUFFER 6
LINE BUFFER 7
506a
506b
506c
506d
506e
506f
506g
502
516
516a
516b
516c
516d
516e
170
GRAPHICS FILTER

FIG. 31

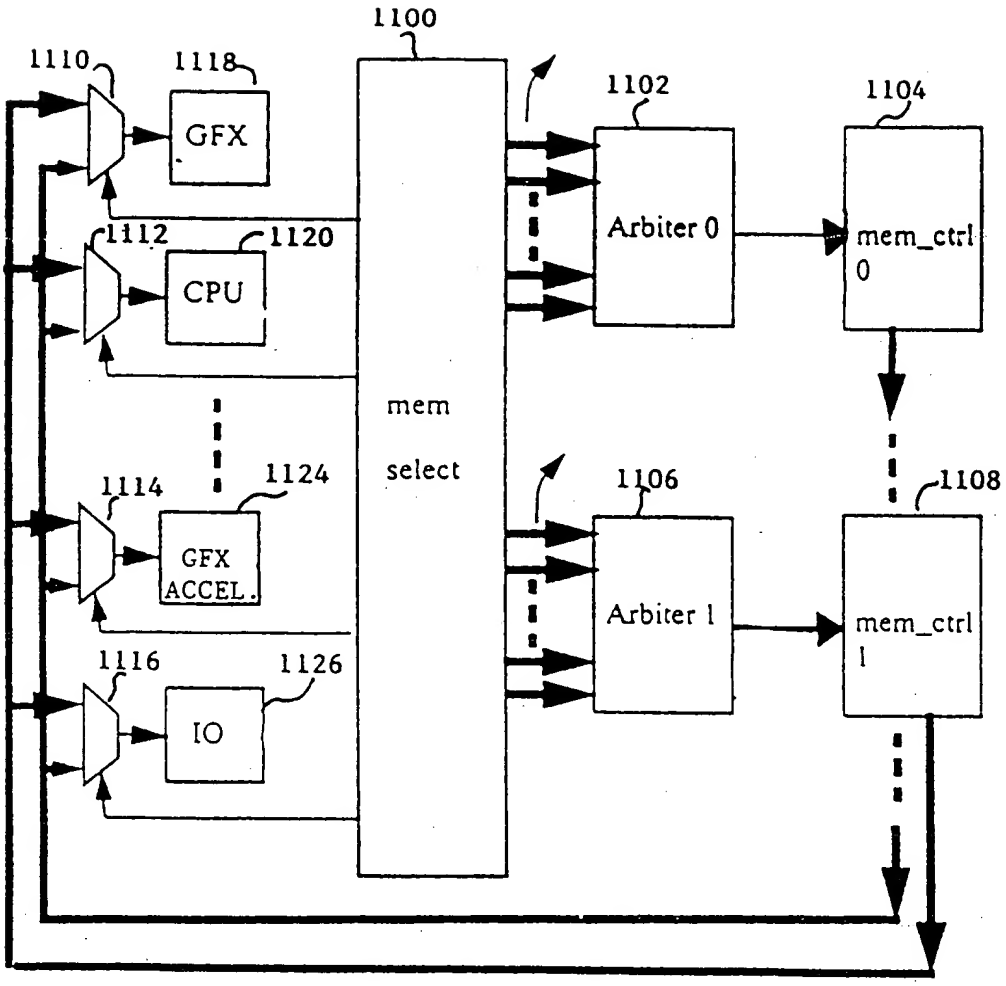
1100
1110
1118
GFX
1102
1104
Arbiter 0
mem_ctrl
0
1112
1120
CPU
mem
select
1114
1124
GFX
ACCEL.
1106
1108
Arbiter 1
mem_ctrl
1
1116
1126
IO

FIG. 32

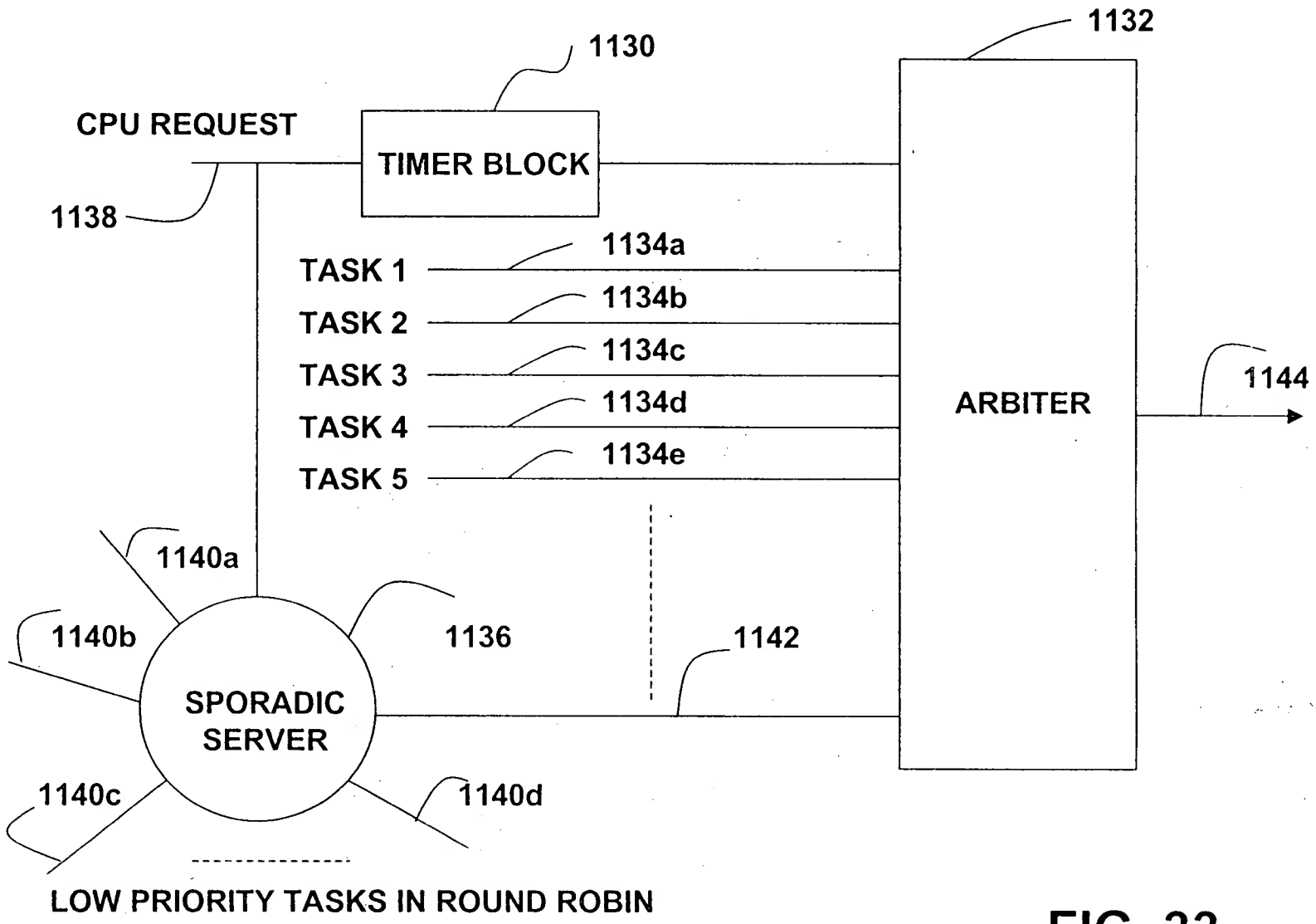
1132
1130
CPU REQUEST
TIMER BLOCK
1138
1134a
TASK 1
1134b
TASK 2
1134c
TASK 3
1134d
TASK 4
1134e
TASK 5
ARBITER
1144
1140a
1140b
1136
1142
SPORADIC SERVER
1140c
1140d
LOW PRIORITY TASKS IN ROUND ROBIN

FIG. 33

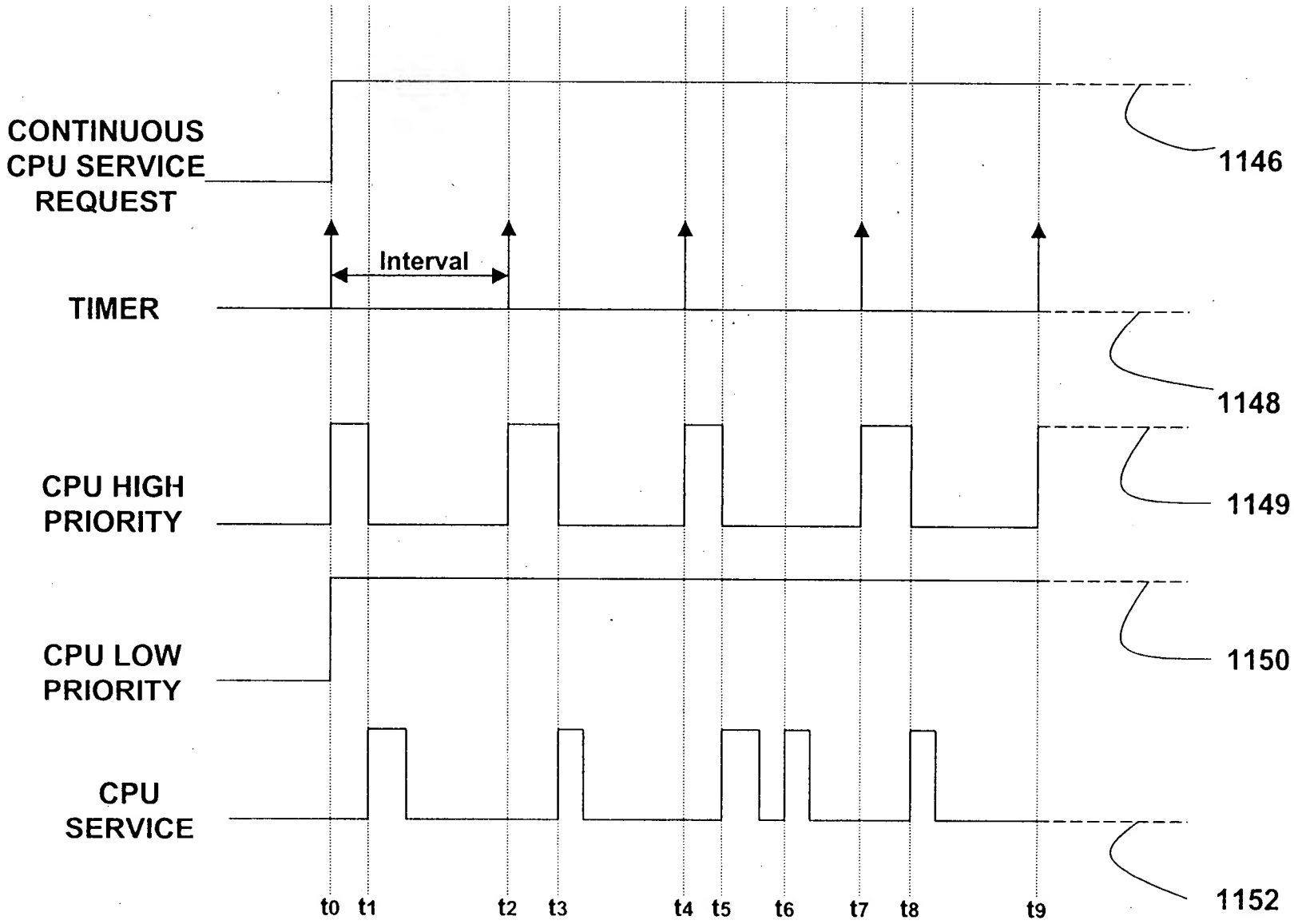
CONTINUOUS CPU SERVICE REQUEST
Interval
TIMER
CPU HIGH PRIORITY
CPU LOW PRIORITY
CPU SERVICE
1146
1148
1149
1150
1152
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9

FIG. 34

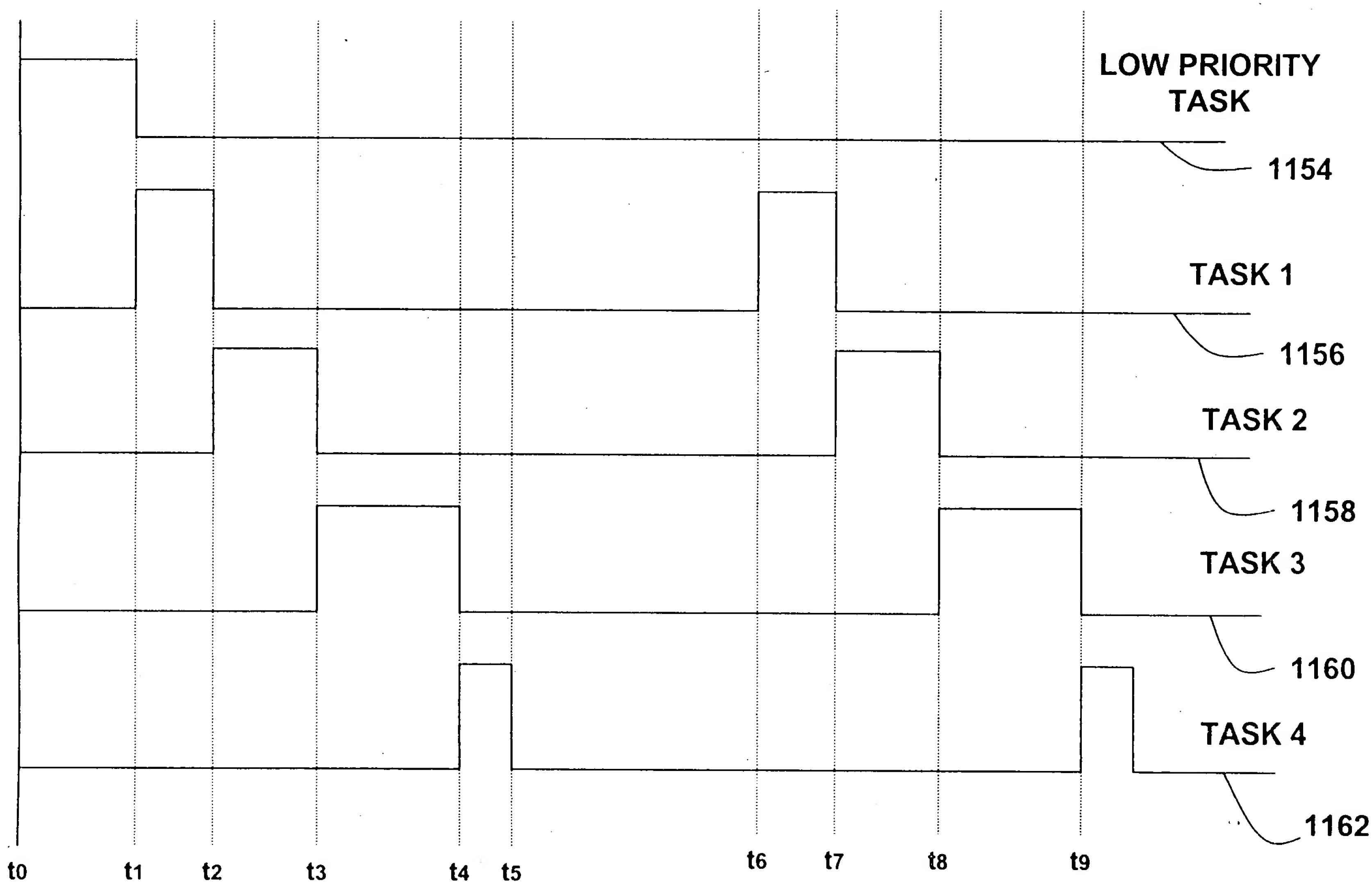
LOW PRIORITY TASK
1154
TASK 1
1156
TASK 2
1158
TASK 3
1160
TASK 4
1162
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9

FIG. 35

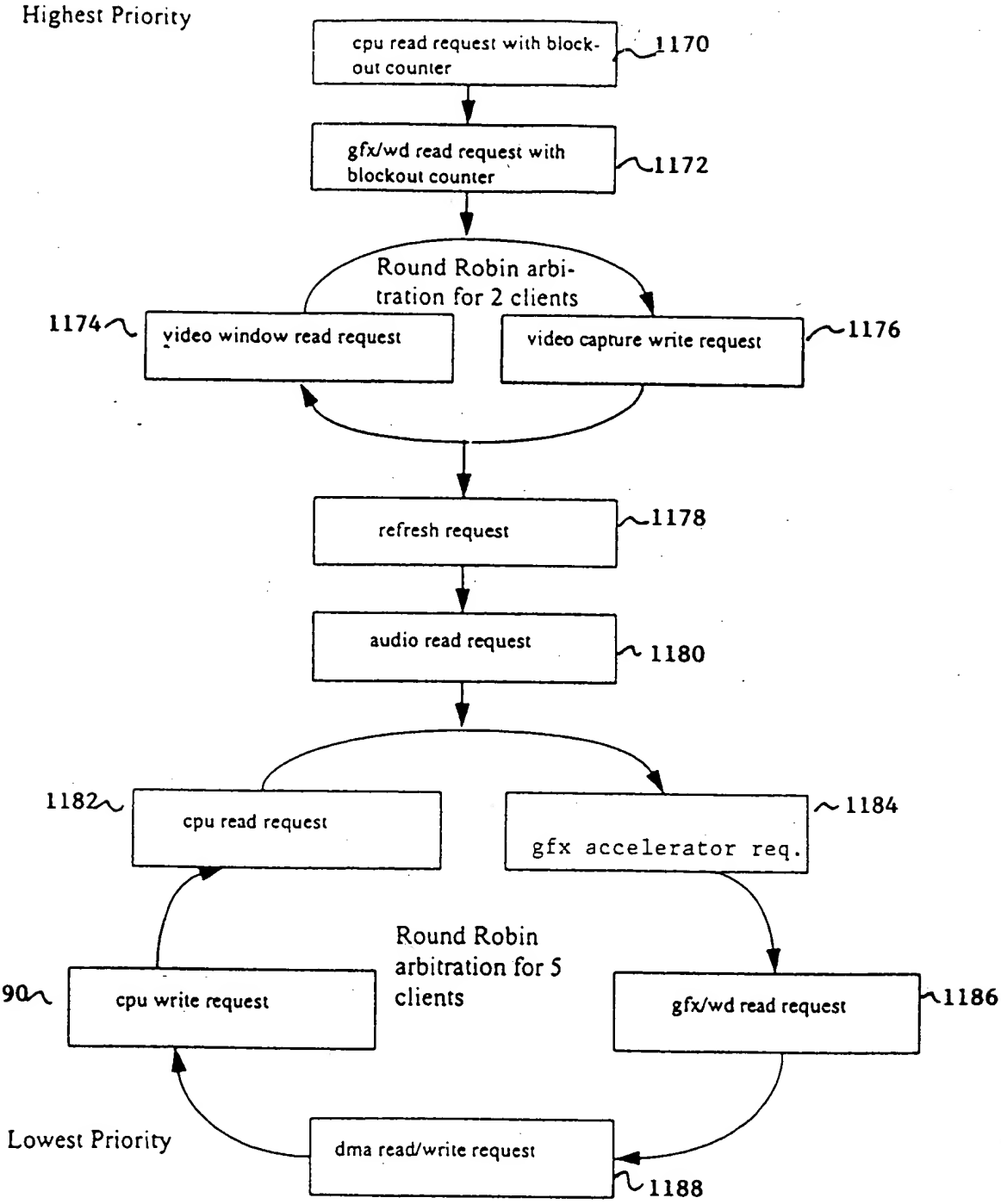
Highest Priority
cpu read request with block-out counter
1170
gfx/wd read request with blockout counter
1172
Round Robin arbi-tration for 2 clients
1174
video window read request
video capture write request
1176
refresh request
1178
audio read request
1180
1182
cpu read request
gfx accelerator req.
1184
Round Robin arbitration for 5 clients
1190
cpu write request
gfx/wd read request
1186
Lowest Priority
dma read/write request
1188

FIG. 36

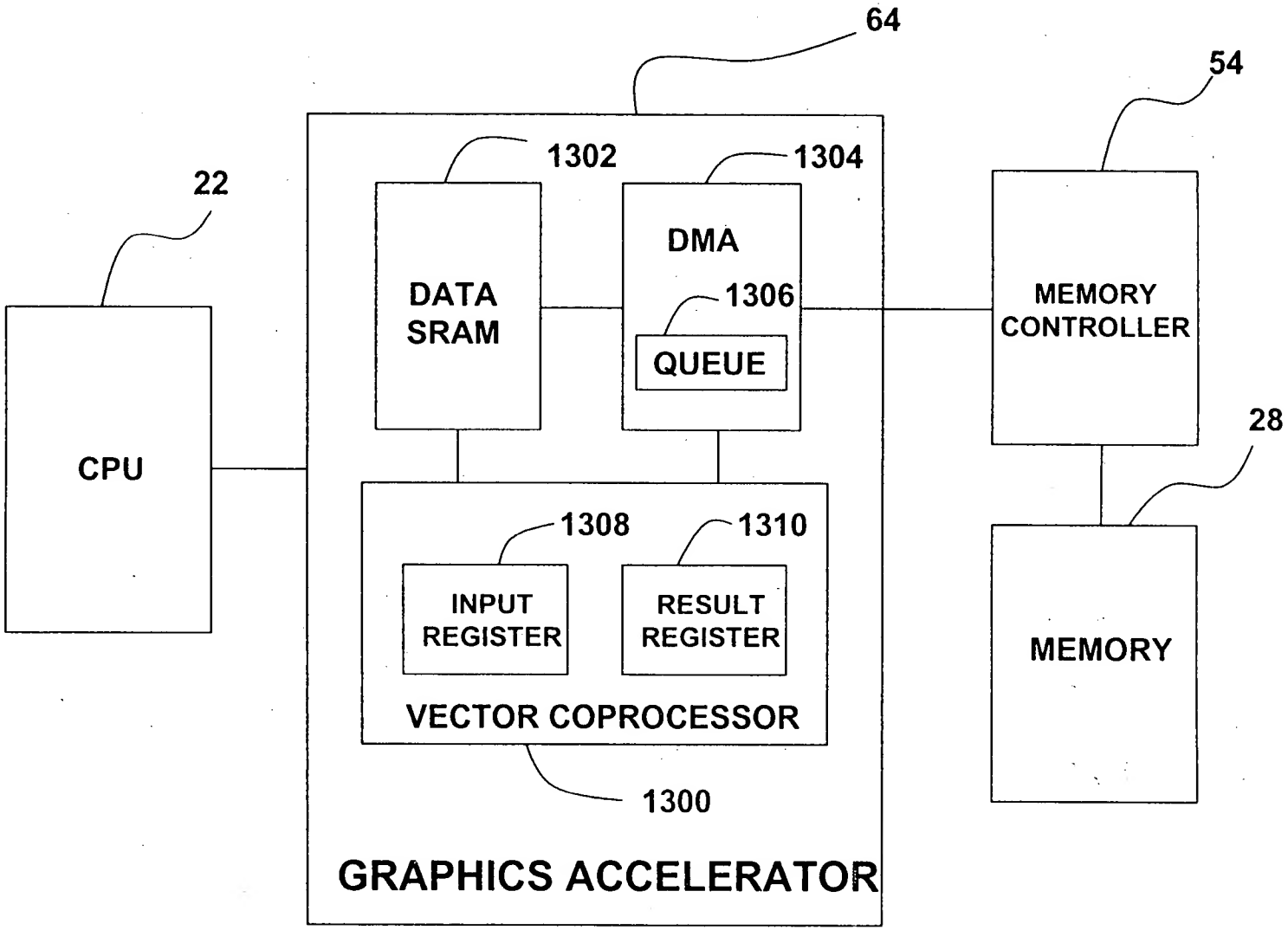
64
54
22
1302
1304
DMA
DATA SRAM
1306
QUEUE
MEMORY CONTROLLER
CPU
28
1308
1310
INPUT REGISTER
RESULT REGISTER
MEMORY
VECTOR COPROCESSOR
1300
GRAPHICS ACCELERATOR

FIG. 37